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DESIGN OF ADDER AND SUBTRACTOR HAVING LESS POWER DISSIPATION

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Abstract: **-With the advancement in technology in the field of digital electronics, reversible logical has become a powerful tool in wide variety of areas like in designing of low power VLSI circuits, DNA computing, quantum computing and optical computing. Circuits made using reversible logic are more energy efficient and consumes less power. In these modern times we need designs of circuits that are speed efficient and should also consume less power. This paper emphasizes on presenting the improved reversible combinational circuit of eight – bit parallel adder and subtractor. These circuits are designed and implemented using Feynman, Double Feynman and MUX gates. Three designs of reversible eight – bit parallel adder and subtractor is proposed. Performance of all three designs is analyzed based number of reversible gates required, garbage input and output, quantum cost.**

Keywords: **Reversible Logic, Binary adder and subtractor, Garbage input and output, Total Logical Calculation**

I. INTRODUCTION

While designing circuits, the most important element that is considered is dissipation of energy. Circuits implemented using reversible logic are more energy efficient. Due to loss of one bit of information, small amount of energy is dissipated.

Heat Dissipation (due to loss of one bit) = kTln(2) where, 'k' is Boltzman constant and T is the temperature.

If reversible gates are use then, energy dissipation can be saved. As in reversible gates we can extract input from the output only.Many arithmetic digital circuits like Adders, Subtractors and MUX hold its importance in computing system. Dedicated Adder/Subtractor circuits are required in a number of Digital Signal Processing applications. So, energy dissipation becomes one of the most important aspects which every designer before designing any circuit takes care. Using reversible gates we can minimize energy dissipation, quantum costs and garbage input/outputs. Three designs of 8-bit binary adder and subtractor using reversible logic gates are designed. Comparison of all three designs is done, in which design III is better among another two in terms of number of reversible gates used, garbage inputs/outputs and quantum cost.

The organization of paper holds section 1 which is introduction. Section 2 is brief overview about reversible gates. Section 3 is the proposed design. Section 4 is about the comparison results. Section 5 is Conclusion and Future Scope and Section 6 is references.

II. REVERSIBLE GATES

Reversible gates are gates which consume their own input and the number of inputs and outputs in these gates are same.Simplest reversible gate is NOT gate. It is 1*1 gate as it has one input and output.

Gate	Quantum Cost
1*1	0
2*2	1

Table 1

NOT Gate: It is 1*1 gate and has quantum cost 0.

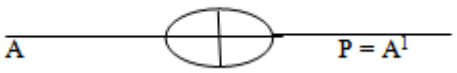

Fig.1

Feynman / CNOT Gate: It is 2*2 reversible logic gate having quantum cost one.

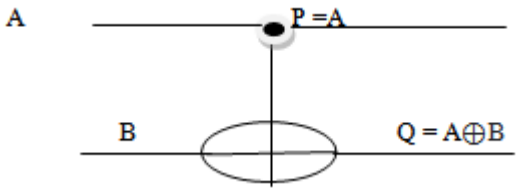

Fig. 2

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Toffoli Gate: It is 3*3 reversible logic gate. It is one of the most popular reversible gates. It has quantum cost of five.

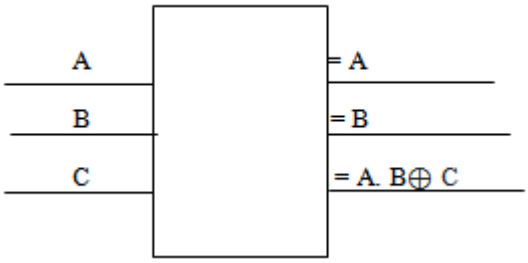

Fig.3 (Toffoli Gate)

Fig. 4 depicts quantum implementation of Toffoli Gate.

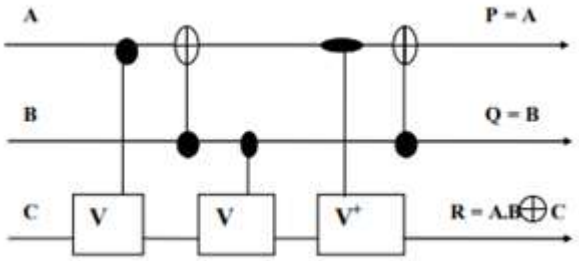

Fig. 4

Peres Gate: It has three inputs as well as three outputs i.e., it is 3*3 reversible logic gate. It has quantum cost of four.

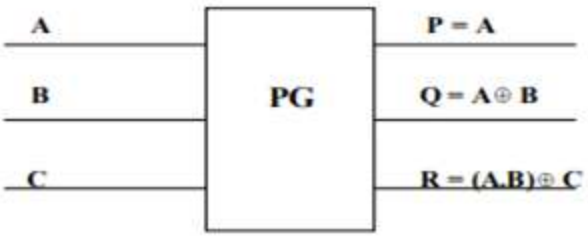

Fig. 5

Fig. 6 depicts quantum implementation of Peres Gate.

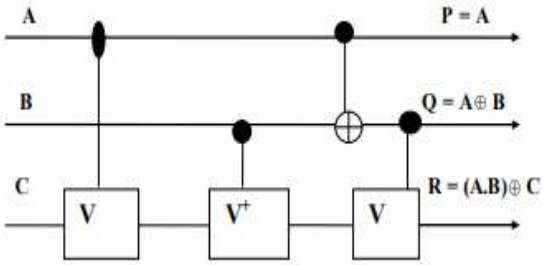

Fig.6

Fredkin Gate: It is 3*3 reversible gate having quantum cost of five.

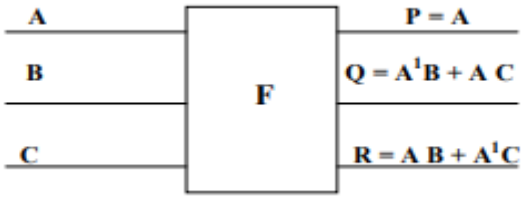

Fig. 7

Fig. 8 depicts implementation of Fredkin gate.

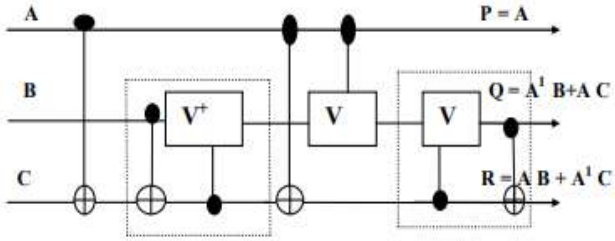

Fig. 8

TR Gate: It is 3*3 reversible gate. Quantum cost of TR gate is equal to six.

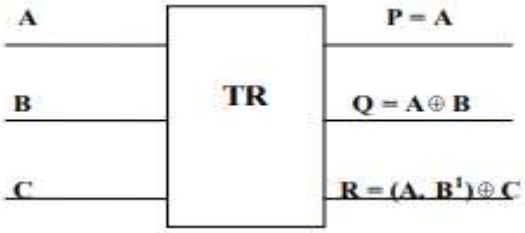

Fig. 9

Fig. 10 depicts the quantum implementation of TR gate.

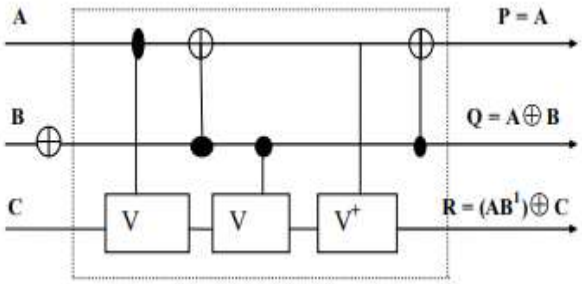

Fig. 10

III. PROPOSED MODEL

Design 1.
Half Adder/Subtractor:

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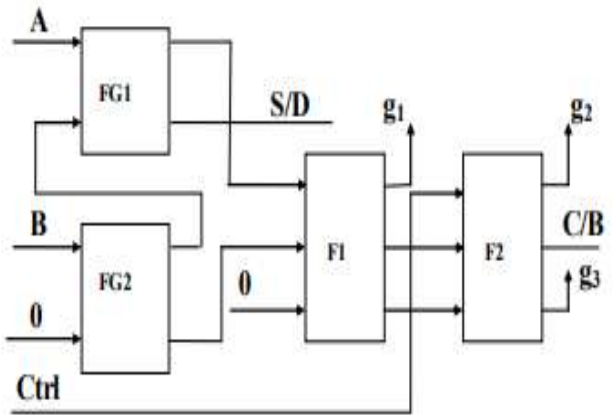

Fig. 11

It is implemented using two FG gates and two F gates. Number of garbage outputs are three while garbage input is two. Quantum cost is twelve.
Full Adder/ Subtractor:

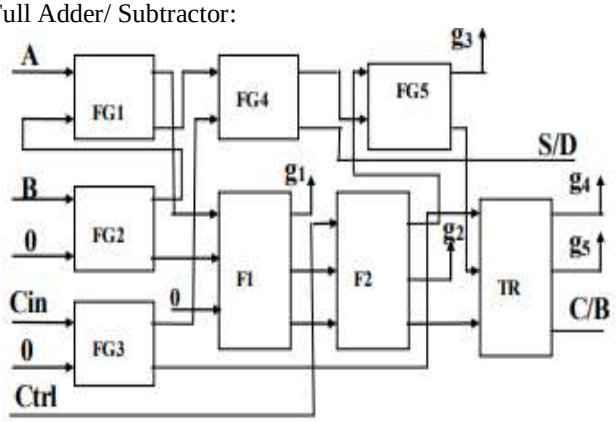

Fig. 12

It is implemented using five FG gates, two F and one TR. Garbage inputs are three while garbage output are five. Total quantum cost of the design is 21.

Design 2.
Half Adder/Subtractor:

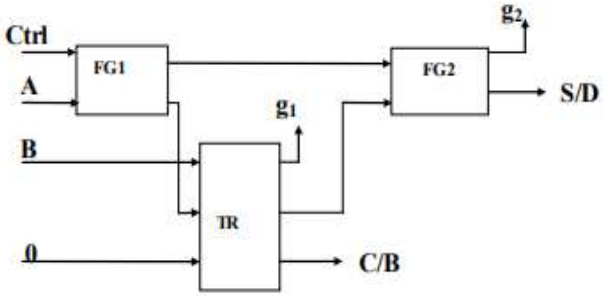

Fig. 13

It is made using two FG gates and one TR gate. Garbage input is one and output is two. Quantum cost is eight.
Full Adder/Subtractor:

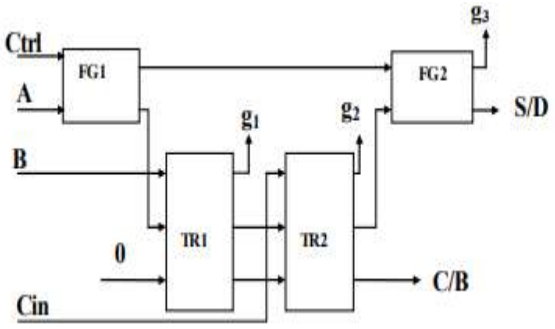

Fig. 14

It is designed using two TR and two FG gates. Garbage input is one and garbage outputs are three. Total quantum cost for design is fourteen.

Design 3.
Half Adder/Subtractor:

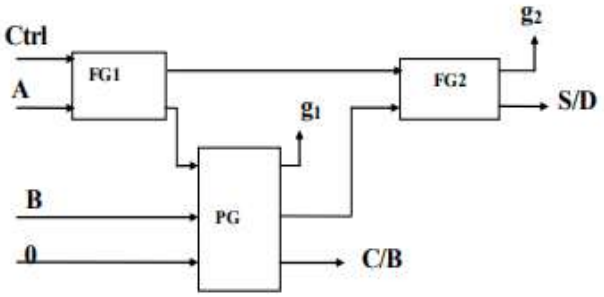

Fig. 15

Two FG and one PG gate is required to implement the design. Garbage input is one and garbage output is two. Total quantum cost is six.
Full Adder/ Subtractor:

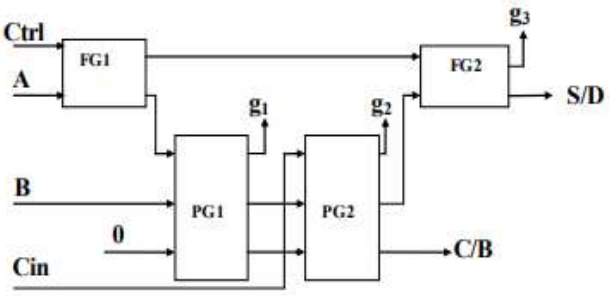

Fig. 16

It is made using two FG and PG gates. The garbage input is one while the garbage outputs are three. Total quantum cost involved in designing is ten.

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Reversibleeight-bit Parallel Binary Adder/Subtractor:

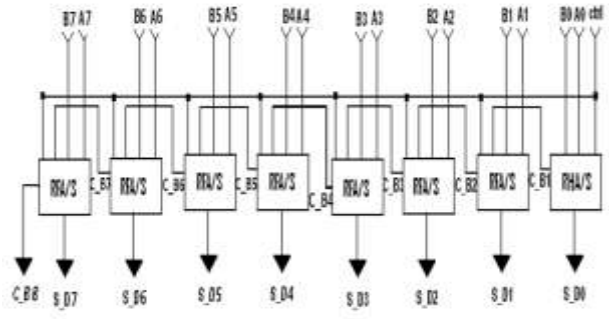

Fig. 17

Reversible eight- bit parallel binary adder/ subtractor are designed using half and full adder/ subtractor that are made in design one, two and three. The addition and subtraction are selected using ctrl input. The input of two eight – bit numbers is given from A0 to A7 and from B0 to B7. While carry/ borrow is shown by C_B1 to C_B7. Addition/ Subtraction output is obtained in S_D0 to S_D7. The eight-bit parallel binary adder/ subtractor is designed using seven full adder/ subtractor and one-half adder/ subtractor. The first stage of diagram represents half adder/ subtractor while rest are full adder/ subtractor.

IV. RESULTS

Comparison of reversible full adder/ subtractor of Design 1, Design 2, and Design 3 are done in various aspects such as number of reversible gates used, number of garbage inputs and outputs and quantum cost involved in designing is shown in table below. It was observed that Design 3 was better as compared to other to. Number of gates in designing is four as compared to Design 1 and Design 2 which uses eight and four gates respectively. Garbage outputs are three and input is one in Design 3, while other two design has input one and output three in Design 2. On the other hand, Design 1 has five garbage outputs and three garbage inputs. Similarly, quantum cost is ten in Design 3 and twenty-one and fourteen in Design 1 and Design 2 respectively.

	Reversible Gates	Garbage Outputs	Garbage Inputs	Quantum Cost
Add/Sub-Design 1	08	05	03	21
Add/Sub-Design 2	04	03	01	14
Add/Sub-Design 3	04	03	01	10

Table 2

Comparison of reversible eight- bit parallel full adder/ subtractor of Design 1, Design 2, and Design 3 are done in various aspects such as number of reversible gates used, number of garbage inputs and outputs and quantum cost involved in designing is shown in table below. It was observed that Design 3 was better as compared to other to. Number of gates in designing is thirty-one as compared to Design 1 and Design 2 which uses sixty and thirty-one gates respectively. Garbage outputs are twenty- three and input are eight in Design 3, while other two design has input eight and output twenty- three in Design 2. On the other hand, Design 1 has thirty-eight garbage outputs and twenty- three garbage inputs. Similarly, quantum cost is seventy-six in Design 3 and one hundred and fifty-nine and one hundred and six in Design 1 and Design 2 respectively.

	Reversible Gates	Garbage Outputs	Garbage Inputs	Quantum Cost
Add/Sub-Design 1	60	38	23	159
Add/Sub-Design 2	31	23	08	106
Add/Sub-Design 3	31	23	08	76

Table 3

Simulation Result of Reversible half adder/ subtractor is given in fig. 18

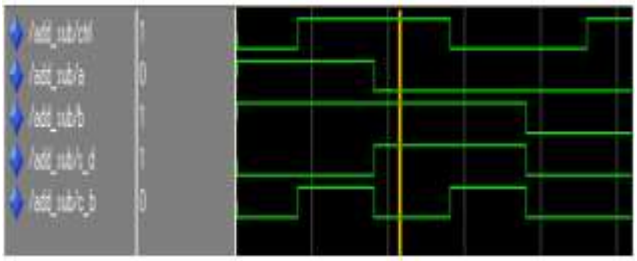

Fig. 18

Simulation result of Reversible full adder/ subtractor is given in fig. 19

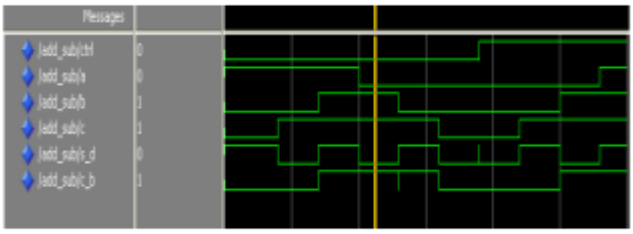

Fig. 19

Simulation result of Reversible eight-bit parallel binary adder/ subtractor in fig. 20

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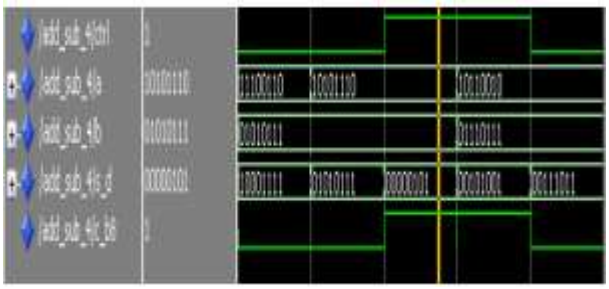

Fig. 20

V. CONCLUSION AND FUTURE SCOPE:

The Reversible gates are used to implement Full Adder/Subtractor and Reversible eight-bit Parallel Binary Adder/Subtractor. In this paper, we proposed Reversible eight-bit Parallel Binary Adder/Subtractor unit. The Design 1, Design 2 and Design 3 are used to implement half and full Adder/Subtractor. The Reversible eight-bit Parallel Binary Adder/Subtractor is built using three designs. The Design 3 implementation of Reversible eight-bit Parallel Binary Adder/Subtractor has better performance as compared to Design 1, Design 2 and existing design in terms of number of gates used, Garbage inputs/outputs and Quantum Cost, hence can be used for low power applications. Existing design requires more than eighty gates to build eight-bit parallel adder/ subtractor while Design 3 only needs thirty-one gates which does not only lower gates count but also reduce quantum cost, power dissipation and increase computational speed too. In future, the design can be extended to any number of bits for Parallel Binary Adder/Subtractor unit and also for low power Reversible ALUs, Multipliers and Dividers.

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