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DEVELOPMENT OF EMBEDDED WEB SERVER CONFIGURED ON ZCU102 FPGA USING SOFTCORE PROCESSOR

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***Abstract*— The most recent developments in Very Large Scale Integration (VLSI) design is Multiprocessor systems-on-chips (MPSoC's), MPSoC's are heterogeneous processors and provide the flexibility of using both on-chip and off-chip memory. Due to the increasing demands for low power operations, fast processing and rich set of peripherals makes MPSoC design an important field of research. In this paper, Zynq MPSoC FPGA based web server application is developed using UART serial interface, Ethernet interface, GPIO's and SD interface for file read/write operation. The Zynq Ultrascale+ MPSoC is first all programmable MPSoC which is a pre-tested and pre-designed intellectual property (IP's) and can be synthesized on FPGA. An embedded system is the combination of both hardware and software platforms. It is very hard to develop an embedded system because of its fixed constraints like power consumption, size, area and cost. Therefore, use of Zynq MPSoC processor is the best solution to design an embedded system. In this paper, Zynq Ultrascale+ MPSoC processor based web-server application is developed on ZCU102 platform using TCP/IP stack and HTTP application protocol at port 80.**

Keywords*— *Web-server, ZCU102 FPGA, Zynq UltraScale+ MPSoC, TCP/IP protocol

I. INTRODUCTION

An integrated circuit which can be configurable by the customer to perform a specific task are called as Field Programmable Gate Arrays (FPGA). Due to the recent development on FPGA and high demands on portable devices, optimization in various aspects is required based on target application since they provide both performance of ASICs and flexibility of software processors. The advantage of parallel processing can be added to FPGA when custom logic design is added to the control systems.[5] and which is not available in embedded systems which works sequentially.

The Zynq UltraScale+ MPSoC is one of the family of Xilinx UltraScale+ MPSoC architecture and it is shown in fig. 1. The UltraScale+ MPSoC family has a quad-core ARM Cortex-A53 with 64-bit and dual-core ARM Cortex-R5with 32-bit based processing system (PS) and Xilinx programmable logic (PL) which is integrated into a single device. The ARM Cortex-A53 is the heart of the Zynq processing system and includes on-chip memory, multiport external memory interfaces, and a rich set of peripheral connectivity interfaces [6].

Embedded system is the fusion of both hardware and software components intended to work together and provide optimized design in order to decrease the size and cost of the product and increase the reliability and performance. They are the tiny part of well-built devices or machines[3]. They provide a wide range of applications in the fields like consumer electronics, industrial, automotive, data centers, medical, commercial and military applications. The hardware and software platform architecture will be based on Xilinx multiprocessor technologies and solutions are exploited by the features of Xilinx's Zynq MPSoC FPGA[5].

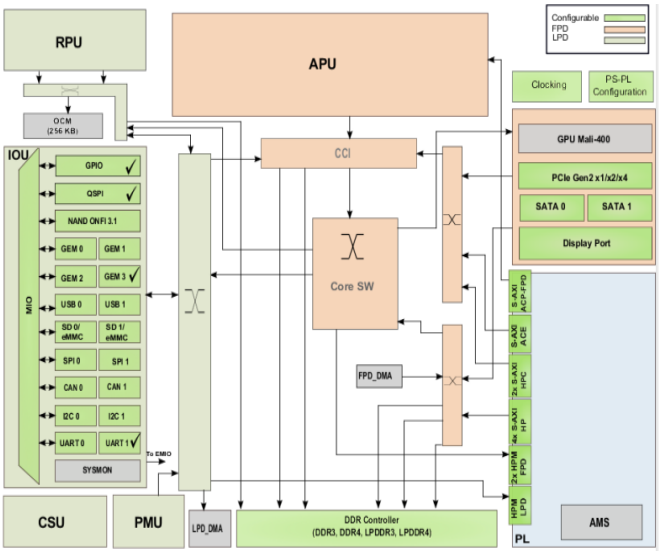

Figure 1. Zynq UltraScale+ MPSoC architecture

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II. OBJECTIVES

This paper describes an approach for the development of web-page for controlling GPIO's using an FPGA based web server implemented on a Zynq MPSoC FPGA, which involves Client-Server architecture. The open source Light weight IP (LwIP) standalone TCP/IP protocol stack is used to implement networking capability and the FPGA based web server enables to access the control system by using a web browser to send the information and updates the system. Ethernet is selected as the fundamental IP for our design since most of FPGA includes an MAC (Ethernet Media Access Controller) that allows direct, data link level contact to the PHY(physical layer) of on-board chip. For effectively implementing this solution, our efforts have targeted:

- Configuration of UART, GPIO's, SD controller for storing the files and displaying the information.
- Enabling of GEM controllers as an HDL IP Core for Ethernet communication.
- The development of a software application that communicates with the embedded GEM controller on the FPGA over the Ethernet, using a TCP/IP protocol over the data-link layer.
- Abstracting away the density of using the software application by implementing a web server application for transferring data to/from the FPGA using a web browser and HTML web page as an interface to the user.

III. RELATED WORK

In [1], developed an Zynq Soc FPGA Based Web Server for Real-Time Remote Control and monitoring .In this client-server architecture is designed and Light weight IP(LwIP) is used to implement the networking capability on TCP/IP stack to control the real-time traffic light. Real-time traffic light is controlled using FPGA based web server by enabling access to web browser to transfer the information and updates the system with new data.

In [4], proposed an approach for the development of embedded web server using soft core processor. In this approach ,the design aims such that web server is capable of adapting multipurpose operation and can monitor the devices placed in remote place through this application using Real Time Operating System(RTOS) on soft core processor. Developed design is tested on NIOS II Soft core processor of DE2 Board.

In [14], proposed an Implementation of Ethernet Based Data Transfer Using FPGA. In this approach after establishing link between PC and ML507 Board, Ethernet packets can be received, can extract the actual data, process the data and finally transfer to other systems if necessary. The design is implemented on Virtex-5 ML507 FPGA and processor is configured in SDK (Software Development Kit).The SCD (System Controller Display) sends the commands to the board and the output is given to the GPIO Pins.

IV. SYSTEM DESIGN ANDIMPLEMENTATION

The embedded web server application based FPGA is developed using Xilinx ZCU102 evaluation board. Web server is the software or hardware mechanism used to run the specified software which satisfies the user requirements and only restricted resources can be accessed. The Zynq Ultrascale+ MPSoC processor is configured such that it provides Ethernet communication between the PC and ZCU102 board and required I/O peripherals like UART, SD, GPIOs and GEM IPs are enabled for successful communication. The Ethernet port of the ZCU102 board is configured with an IP address 192.168.1.10 and EMAC address. The developed embedded system is controlled and monitored by connecting it to the PC through Ethernet cable. User can send commands to ZCU102 board using POST commands to monitor the GPIO's, reading into DDR memory and writing on DDR memory. Upon receiving submit command from the user, the browser available on PC updates the values on web page to monitor the GPIO's. SD interface is also used in this design to provide file transfer to and from the PC using SD mode.

The block diagram of the developed system is shown in fig. 2. The Zynq Ultrascale+ MPSoC processor is binded to the TCP/IP stack at port 80 and web server application is designed on ZCU102 board using HTTP application-level protocol.

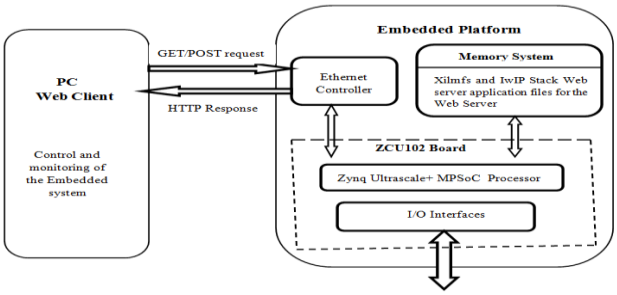

Figure 2. Block diagram of proposed system

TCP/IP stack can be programmed in two methods and the two methods are Socket API, RAW API.

The socket method is very slow because it blocks on each phase of socket read and write operations until they are complete which causes the overhead of all other operations and also requires many pieces to complete the task.

Whereas the RAW method is very fast because operations are performed in call-back technique. Applications that employs RAW method schedules the call-back functions on particular tasks like read, write, accept, request and all operations are performed in call-back technique.

In our design we have adopted the RAW method to develop the web server based application using LwIP TCP/IP protocol. The main function of web server is to store, develop and send web pages to the users. Such web server can be used to control and monitor an embedded system via available

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browser. The web server application developed would perform the following tasks:

- To obtain the files which are in the memory file system of ZCU102 board using HTTP GET command.
- Monitoring the status of LEDs of ZCU102 board using HTTP POST command and output the corresponding hexadecimal value onto the web page.
- Transfer of data through the ZCU102 board and display it on UART terminal.
- Retrieve the position of pushbutton switches from the ZCU102 board using HTTP POST command and display its corresponding binary value onto the web page.

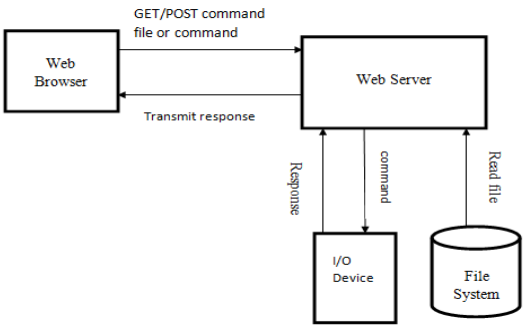

Figure 3. Communication between User and Server

V. SOFTWARE/HARDWARE SPECIFICATION

A. Tools Used

- Xilinx Vivado Design Suite
- Software Development Kit(SDK)
- Teraterm Terminal

B. Software Specification

The Vivado design suite is a platform used for high-level synthesis and analysis of Hardware Description Language (HDL) designs. It is the latest version of Xilinx with some extra features for SoC enhancement. The complete design can be re-written and it includes in-built logic simulator.

Software Development Kit (SDK) is a program which allows C/C++ programming for the Zynq Ultrascale+ MPSoC processor. It uses GNU C complier, which is the earliest application to distribute true homogeneous and heterogeneous multiprocessor designs, debug and analyse the performance parameter.

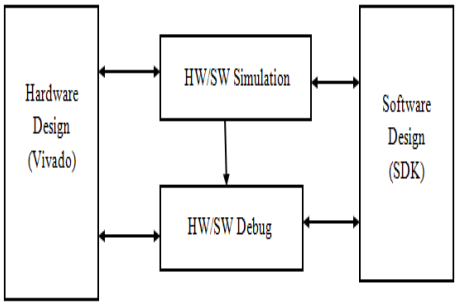

Figure 4. Hardware Software Co-Design

C. Ethernet Interface

Wired local area networks (LANs) can be connected using Ethernet that enables devices to communicates with each other using TCP/IP protocol. Once the connection establishes between PC and ZCU102 FPGA board, transfer of packets takes without any loss as shown in fig.5.

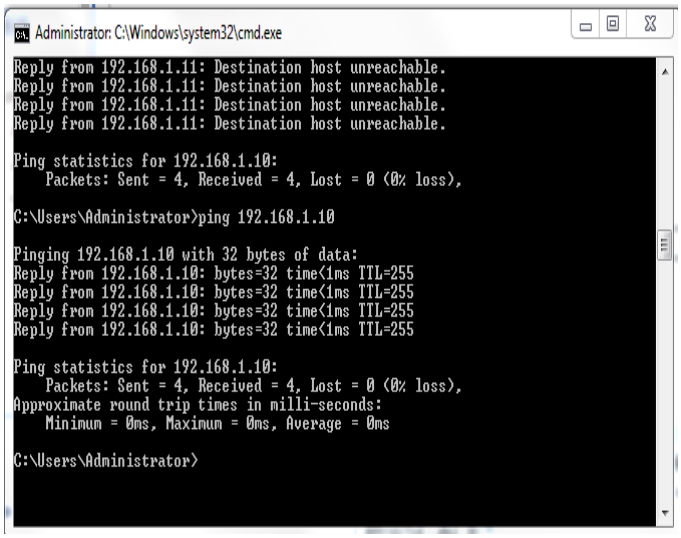

Figure 5. Connection between PC and Board

D. UART Interface

The operations of UART are controlled by configuration and mode registers. The configuration parameters are data bits, stop bits, baud rate, parity bit and character spacing. In modern days, external USB to UART bridges are commonly used which combines the hardware cables and a chip to perform USB to UART conversion. In this design UART is implemented to display the data received on Ethernet port and baud rate of 115200 is used. The encapsulated data is transmitted on transmitter pin(TX) of the bridge communication. After transmitting, the data undergo an ASCII conversion and it is displayed on the PC terminal.

E. SD Card Interface

SD card is a type of non-volatile memory used to provide high-capacity memory in a small volume. The FAT file system defined for SD card is used for storing the files. SD

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card uses FAT12/16 for 2Gbyte and lower rates and FAT32 for 4Gbytes and higher rates. The default mode for SD card is SD mode but the SD card can be configured to much slower or any other modes. In this design file is created in SD card, some required data is written into the file and the data can be accessed through SD mode.

F. Web-Server Flow chart

Web server is the software or hardware technology that is used as an intermediary between Zynq Ultrascale+ platform and the web client. The major task of a web server is storage purpose, process and delivery of web pages to clients. Light weight IP (LwIP) standalone TCP/IP stack is used to implement networking capability and the FPGA based web server enables to use the control system by using a web browser to send the data and updates the system. The communication between web client and web server is done through HTTP protocol based on request commands.

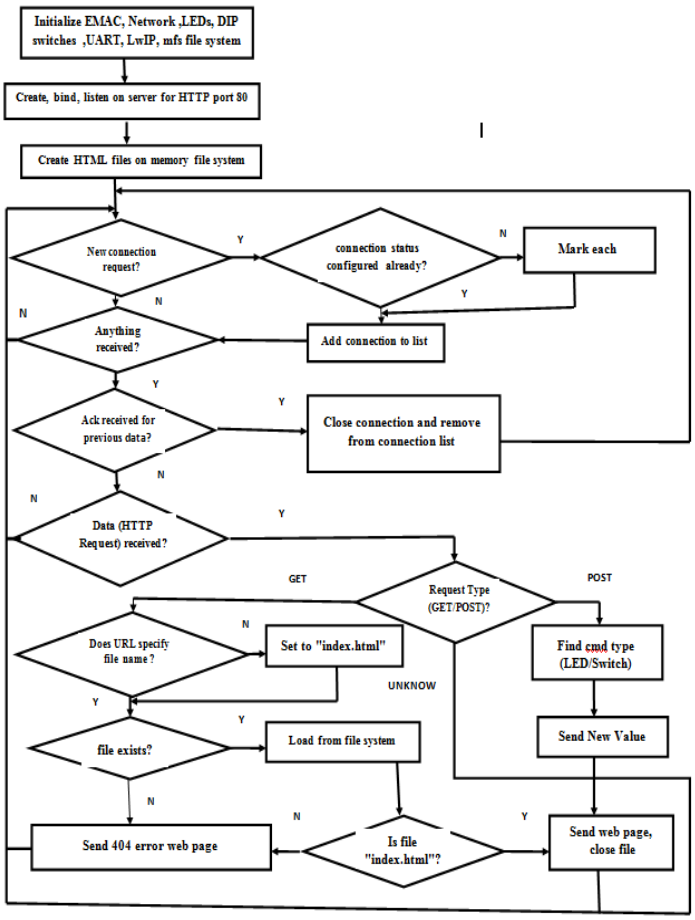

Figure 6. Web server Flow Chart

In Web-server application, the required peripherals like Ethernet(GEM), UART, SD, GPIO's are enabled in Vivado block design and bitstream is generated for the same. SDK is launched for the corresponding design where the IP's like LwIP and xilmfs is configured and binded to port 80 of HTTP protocol. The developed html file is converted into mfs file format and stored onto memory file system. Run the application and check for the connection. If connection is established, it checks for index.html file on memory file system. If index.html is present then point to the URL to open the web page or else sends error message like index.html is not present on memory file system. The above mentioned procedure is explained in flow chart manner in fig.6.

VI. RESULTS

Table 1 : Device Utilization Summary

On Chip	Power (W)	Used	Available	Utilization (%)
Look up tables	0.002	971	274080	0.35
LUT as Shift Register	<0.001	42	144000	0.03
Distributed RAM	<0.001	56	144000	0.04
Register	<0.001	1175	548160	0.21
I/O Signals	0.001	9	328	2.74

Table.1 depicts the device utilization summary of the block design. Here, the results of web-server application is explained sequentially. Instantiates required IP cores in Vivado and run the web-server application in SDK. On successful operation, the PHY is linked to default IP address *192.168.1.10* of the board and binded to TCP stack at port 7. The data entered will be echoed back at serial ports like teraterm, hyper-terminal, and SDK terminal. The corresponding results observed in Teraterm are shown in fig.7.

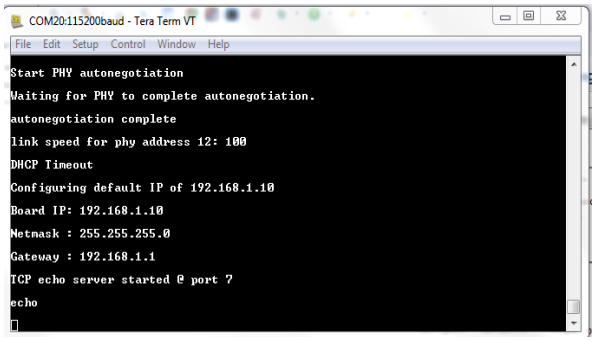

Figure 7. TCP stack connection

The fig.8 depicts the results of MFS file creation of index.html which is present on memory file system. Use the below command to create MFS image.

mfsgen -cvbf image.mfs 400 index.html

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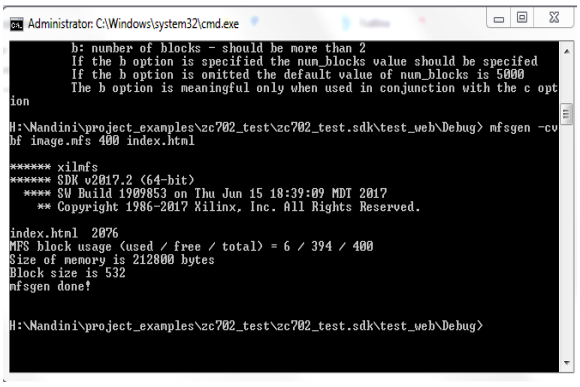

Figure 8. MFS image creation

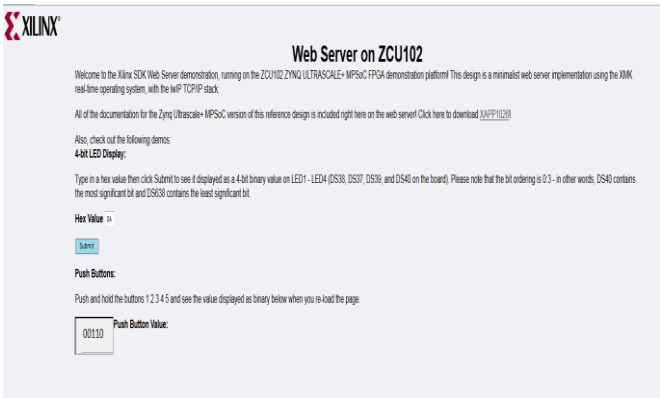

Figure 9. Designed Web page for GPIO's

The web page is created for the web-server application to control the GPIO's of the ZCU102 board is shown in fig.9. In this web page development, we tried to control the GPIO's like LED and pushbutton. To toggle the LEDs, Hexadecimal value should be entered into web page, the corresponding LEDs will blink accordingly shown in fig.10. By pressing the Push buttons, the corresponding binary equivalent value will be displayed on web page as shown in fig.9.

In Fig. 10, highlighted information depicts the resultant results for the developed application. Where Hexadecimal value **0A** is submitted then corresponding LED's are toggled and Pushbuttons **2** and **3** is pressed and the corresponding binary value **00110** is updated on web page.

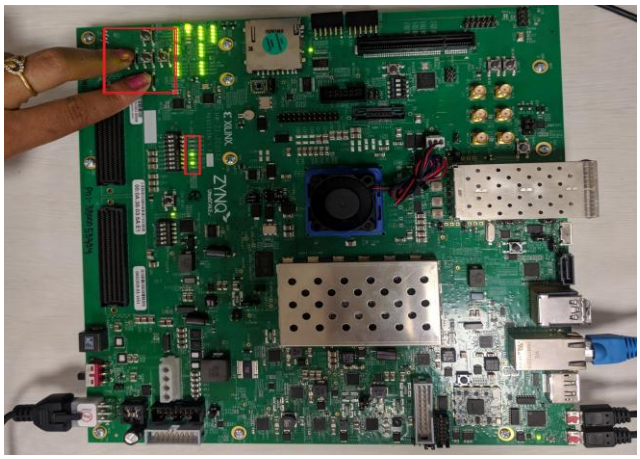

Figure 10. Board results corresponding to web page

VII. CONCLUSION

This paper successfully demonstrates the implementation of embedded web server application on ZCU102 evaluation platform, where we successfully instantiated the IP cores of UART, GEM, GPIO's and SD card interfaces. The targeted application is to control the GPIO's like LEDs and pushbuttons through developed web page. The proposed methodology for web-server application in fig.6 worked very effectively, We observed that device utilization (in table.1) like look-up tables, registers, I/O signals used is very minimal compared to[3]. As a future work, the Web-server application development can be extended further to control& monitor the other Peripherals on ZCU102.

VIII. APPLICATIONS

- The developed web-server application can be used for real-time monitoring systems where client-server architecture is present.
- The web-page can be designed to store the real-time data to access and file transfer between client & server.

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