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ANALYSIS OF SWITCHED CAPACITOR MULTILEVEL INVERTER USING ALTERNATIVE PHASE OPPOSITION DISPOSITION PWM TECHNIQUE FOR VARIABLE FREQUENCY DRIVES

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Abstract— **Using parallel-series converter in as DC Power supply appliance gives a good opportunity to maintain stable supply while the load is changing. In this work, a new step up switched capacitor multilevel inverter is proposed. It consists of two parts such as a switched capacitor circuit and a full bridge inverter which are connected in parallel. Here a small input voltage can be used to produce a boosted output voltage. Number of switches used is very less compared to the conventional inverter. The multilevel dc output voltage of the circuit in the first part becomes the input of the circuit in the second part, resulting in a stepped voltage waveform. Such waveform is close to a sinusoidal and its harmonic content also very less compared to the conventional multilevel inverter by using the Alternative Phase Opposition Disposition (APOD) PWM control strategy. This inverter outputs larger voltage than the input voltage by switching the capacitors in series and in parallel. The maximum output voltage is determined by the number of the capacitors. Unlike the conventional inverters, this topology does not uses a complicated control scheme or isolated dc sources. Also output frequency can be varied by varying the modulating signal frequency. In this paper, the circuit configuration, the theoretical operation, the simulation results with MATLAB/SIMULINK.**

Keywords— **Multilevel Inverter, charge Pump, Charging, Single DC Source, Switched Capacitor**

I. INTRODUCTION

In recent years, a power electronic system plays a important role in many areas of developing fields. With the sudden changes in electric fields, the power electronic devices are expected to handle the higher rating of voltage and capacity [1]-[4]. As a solution to this issue, multilevel inverters have gained much attention in recent years due to its several advantages.

Multilevel inverters produce a stepped output phase voltage with a refined harmonic profile when compared to a two-level inverter [1]. The concept of multilevel inverters, introduced about 30 years ago [1], entails performing power conversion in multiple voltage steps to obtain improved power quality, lower switching losses, better electromagnetic compatibility and higher voltage capability. Nowadays, there exist three commercial topologies of multilevel voltage source inverters: the most popular being the diode-clamped, flying capacitor and cascaded H-bridge [2] [4] structures. These inverters with multiple numbers of levels are more efficient than the two level inverter. But at the same time it has some drawbacks like more no of switching devices, cost etc. Some of the other topologies like the conventional H- bridges use multiple numbers of dc sources to obtain large number of levels in the output.

The diode clamped or neutral point clamped has the difficulty of increase in the number of clamping diodes as level increases. Similarly, in case of flying capacitor multilevel inverter the number of capacitors increases and system becomes bulkier. Among these inverter topologies, cascaded multilevel inverter reaches the higher output voltage and power levels, and the higher reliability due to its modular topology and the simplicity. In all the above topologies, the peak amplitude value of the output will be only the source voltage, with the rest of the levels being only a fraction of input voltage. An advantage of multilevel inverter is the harmonic reduction in the output waveform. As the number of levels increases, the output THD reduces. The multilevel inverter has lesser harmonics compared to the conventional two level inverter. In normal condition when amplitude modulation index is one that time magnitude of output voltage of inverter is same as input voltage. So that we have to use dc/dc boost converter to increase output voltage levels to ensure output voltage is to be

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greater or at output side we have to use inductors or transformer but at higher power transformer should withstand heavy magnetic core so that it can sustain higher power which increases size of whole inverter assembly.

There issues are considered since battery technologies haven't evolved too much. Almost in every application lead acid batteries have proven their potential at lower cost. By reducing size of inverter assembly we can increase the size of these batteries which are in beneficial to end consumers of such products. As a provision against the issue, a charge pump, which does not have any inductors, is applied to such systems. A charge pump output a larger voltage than the input voltage with switched capacitors. When the several capacitors and the input voltage sources are connected in parallel, the capacitors are charged. When the several capacitors and the input voltage sources are connected in series, the capacitors are discharged. The charge pump output the sum of the voltages of the capacitors and the input voltage sources. However, a charge pump has many switching devices which make the system more complicated.

As a solution for all the disadvantages, a new switched capacitor multilevel inverter is implemented. A switched-capacitor (SC) inverter outputs multilevel voltages with switched capacitors. An SC inverter is similar to a charge pump in the topology. The new boost switched capacitor multilevel inverter produce greater output voltage than the input voltage. It makes use of only one dc source as the input and the number of switching devices is reduced when compared to the widely used conventional topologies. This multilevel inverter does not have any inductors which make the system small. The output harmonics of the novel multilevel inverter are reduced by the multilevel output. Another advantage is the input required to obtain a particular output voltage is very less compared to the existing inverters.

II. CIRCUIT TOPOLOGY OF SEVEN LEVEL INVERTER

A Switched Capacitor network is a cirsuit used to generate a greater voltage waveform [8]. The staircase output voltage generated by this inverter is the output from the full bridge inverter and the input voltage source for the full bridge inverter is the output from the capcitor circuit. Thus output voltage obtained is greater than the input voltage. The switches in the SC network and full bridge inverter are operated in the high switching frequency. A new step up switched-capacitor (SC) multilevel inverter is formed by cascading two parts, a switched capacitor network and a full bridge inverter [6],[7], [8] shown in figure 1.

The basic switched capacitor cell is developed using one capacitor, two switching devices with one diode as shown in figure 2. Each of these cells are connected in parallel with each other to increases the number of levels that is desired in the multilevel output. Each of the cells is made to operate as a parallel-series converter. Each switched capacitor cell is reduced by one switch. When a switch is turned ON, input source and capacitor becomes in parallel and the diode conducts.

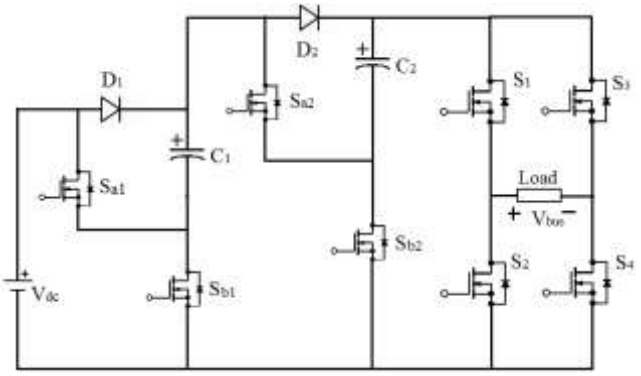

Fig. 1. Circuit diagram of Proposed Seven Level Inverter

. When its turned OFF and complementary switch is ON, the capacitor becomes in series with the input voltage source and the diode is OFF.

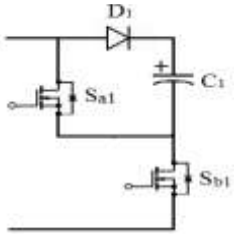

Fig. 2. Switched Capacitor Cell

A voltage source V_{dc} is the input voltage source. By proper switching of the devices the capacitor are charged to the source voltage at first, then for obtaining the required level of output voltage the switches are turned ON and OFF in a way that only the required capacitor becomes in series with the sources and the load.

For N number of cells, the new multilevel inverter generates (2N+3) levels in the output voltage waveform. Number of switches used is very less compared to the conventional inverter.

III. OPERATING PRINCIPLE OF SEVEN LEVEL INVERTER

A switched capacitor seven level inverter is analysed using two SC cells in parallel (N=2). The inverter output voltage is larger than the input voltage by proper switching of SC cells. The capacitors are charged by connecting capacitor and the input voltage source in parallel. And capacitors are discharged when capacitor and the input voltage source are connecting in series. The switching control pulses for the different switches are developed by using the several multi carrier PWM techniques.
The working of inverter can be illustrated by the main three steps;

1. All the capacitors are charged
2. Some of the capacitors are discharged
3. All the capacitors are discharged

The basic operations of the inverter are used to obtain a positive and negative cycle for the multilevel output. The positive half cycle is obtained with switches S_1 and S_4 of full bridge inverter ON and negative half cycle with switches S_2 and S_3 of inverter ON.

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A. ***Mode 1 (V_{bus} = 0 V)***

Switches S_{b1}, S_{b2} are ON and S_{a1}, S_{a2} are OFF. Diodes D_1, D_2 conducts during this period. All capacitors are in parallel with input as shown in figure 3. Switches of the full bridge inverter of the same upper/lower limb conducts.

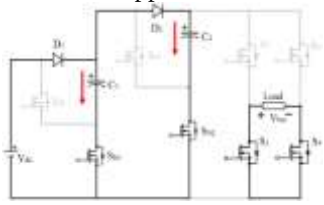

Fig. 3. Mode 1

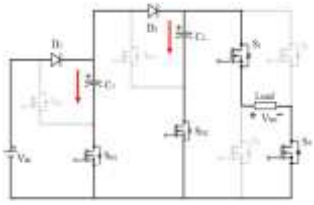

Fig. 4. Mode 2

B. ***Mode 2 ($V_{bus} = V_{dc} - 2V_f$)***

Switches S_{b1}, S_{b2} are ON and S_{a1}, S_{a2} are OFF. Diodes D_1, D_2 conducts during this period. All capacitors are in parallel with input. Switch S_1 and S_4 of the full bridge inverter conducts as shown in figure 4.

C. ***Mode 3 ($V_{bus} = V_{dc} + V_{C1} - V_f$)***

Switches S_{b1}, S_{b2} and S_{a2} are turned OFF and S_{a1} is ON. Switches S_1 and S_4 of full bridge inverter are ON. As a result $C_1$is in series and C_2 is in parallel as shown in figure 5.

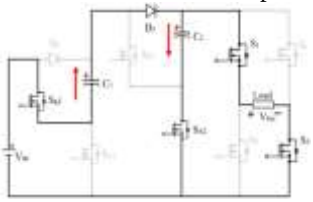

Fig. 5. Mode 3

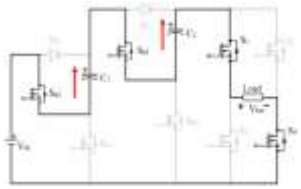

Fig. 6. Mode 4

D. ***Mode 4 ($V_{bus} = V_{dc} + V_{C1} + V_{C2}$)***

In this mode all the capacitors are connected in series. The capacitor C_1 and C_2 are connected in series with the source voltage as shown in figure 6. This is obtained by switching OFF S_{b1}, S_{b2} and simultaneous turning ON of switches S_{a1} and S_{a2}. The switches S_1 and S_4 of full bridge inverter are conducting in this period.

Similarly the negative half cycle can be obtained by turning on S_2 and S_3 instead of S_1 and S_4, thus seven level output can be obtained.

IV. SYSTEM ANALYSIS

A. Number of Levels and Maximum output value

The maximum output voltage level is determined by the number of switched capacitor cell connected to the network. If 'N' is the number switched capacitor cells, then number of output level and maximum output value is given by the relation

No. of output levels, m = 2N+3 (1)

Maximum output voltage = $(N+1)V_{dc}$ (2)

B. Voltage stress across the Switches

The maximum voltage dropped is the output voltage which is across the full bridge switches (S_1, S_2, S_3 & S_4) and minimum voltage dropped is across the switches in the switched capacitor cell. If N is the number of SC cells;

Voltage stress across the full bridge switches (S_1, S_2,S_3 & S_4)

$$V_{fullbridge} = (N+1)\, V_{dc} \quad (3)$$

Voltage across the switches in SC network,

Voltage across switch S_{a1}, $V_{sa1} = V_{dc}$ (4)

Voltage across switch S_{b1}, $V_{sb1} = V_{dc}$ (5)

Voltage across Switch S_{a2}, $V_{sa2} = V_{dc} - V_f$ (6)

Voltage across Switch S_{b2}, $V_{sb2} = V_{dc} + V_{c1}$ (7)

Where, V_{dc} is the input DC voltage

V_f is the forward voltage drop of diodes

N is the number of switched capacitor cells

C. Voltage across the Diodes

Proposed inverter uses double number of diodes compared to the existing topology [3][4]-[9]. In which diodes in the upper limb of the SC cell undergoes high frequency switching and diodes in the lower limb of SC cell undergoes normal switching with different reverse biased voltages. All diodes are forward biased when common switch S_b is turned ON.

Diode D_1 in the upper limb of SC cell is reverse biased by the capacitor voltage when switch S_{a1} is turned ON and Diodes in the lower limb is reverse biased when the common switch S_b is turns off.

Diode D_1 in the upper limb, $V_{D1} = - V_{c1}$ (8)

Diode D_2 in the lower limb, $V_{D2} = - V_{c2}$ (9)

D. Calculation of Capacitors

$$C = \frac{\Delta Q_i}{\Delta V_{Ci}} \quad (10)$$

Where, ΔQ_i Change in charge over a period

ΔV_{Ci} Change in voltage over a period

The required capacitance and voltage ripple are inversely related to each other. An increase in the capacitance will decrease the amount of ripple [3].

$$\Delta V_{Ci} = (\%\ ripple)\ V_c \quad (11)$$

The capacitor C_1 and C_2 are discharged with switching S_{a1} and S_{a2} respectively and capacitance C_i can be calculated as

$$C_i = \frac{\Delta Q_i}{(\%ripple)V_c} \quad (12)$$

E. Switching Angle Calculation

For a multilevel inverter each level is occurred at a particular switching angle. Seven level inverter has three switching angles corresponding to three levels shown in figure 7. For any level inverter switching angles are calculated using the equation (12)

$$\theta_j = \sin^{-1}\left(\frac{2j-1}{m-1}\right) \quad (13)$$

Where, j = 1,2,…….$(\frac{m-1}{2})$

m = output levels

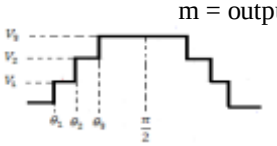

Fig. 7. Calculation of Switching Angles

For the modified Switched Capacitor Inverter V_1=3.4V, V_2=8.4V and V_3=12.6V and corresponding switching angles are θ_1=0.1674rad, θ_2=0.5236rad and θ_3=0.9851rad.

F. RMS Output Voltage

RMS value of the output voltage is calculated using the switching angles of each output step. For the seven level output three switching angles are generated. From results RMS value of output voltage can be calculated using the equation (13)

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$$V_{rms} = \sqrt{\left(\frac{2}{\pi}\right)\left(V_1^{\,2}(\theta_2 - \theta_1) + V_2^{\,2}(\theta_3 - \theta_2) + V_3^{\,2}\left(\frac{\pi}{2} - \theta_3\right)\right)} \quad (14)$$

For the above given values, $V_{rms} = 9.0855V$

RMS value of the fundamental output voltage component can be calculated using the step voltage and switching angle as shown in equation (14)

$$V_{1rms} = \frac{V_1}{\sqrt{2}} \quad (15)$$
$$= \left(\frac{2\sqrt{2}}{\pi}\right)(V_1 \cos\theta_1 + (V_2 - V_1)\cos\theta_2 + (V_3 - V_2)\cos\theta_3)$$
$$= 9.0069V$$

G. Total Harmonic Distortion

The main criterion for assessing the quality of the voltage delivered by an inverter is the Total Harmonic Distortion (THD). The THD is a ratio between the Root Mean Square (RMS) of the harmonics and the fundamental signal.

$$THD = \sqrt{\left(\frac{V_{rms}^2}{V_{1\,rms}^2} - 1\right)} \quad (16)$$

For the Switched Capacitor Inverter, THD = 13.24%

H. Voltage ripple of capacitor

For a switched capacitor cells, when the switch S_{ai} is turned OFF, capacitor C_i (i = 1, 2.....N) starts charging to ($V_{dc} - 2\,V_f$) and when switch S_{ai} turned ON means the charging period of capacitor C_i ends shown in figure 3.

Voltage ripple of capacitor, $\Delta V_c = \frac{1}{C_i}\int_{t_0}^{t_1} i_0\, dt$ (17)

Where t_0 and t_1 are the start and end time of discharging period. For different PWM techniques t_0 and t_1 varies.

$$\Delta V_{Ci} = \frac{1}{2\pi f_s C_i}\int_{\theta_{1+i}}^{\pi-\theta_{1+i}} i_0\; d\omega t \quad (18)$$
$$= \frac{V_{in}}{2\pi f_s R C_i}[\pi - 2\theta_{1+i}] \quad (19)$$
$$= \frac{V_{in}}{2\pi f_s R C_i}\sum_{a=i}^{n}[\pi - 2\theta_{1+i}](a+1) \quad (20)$$

Voltage ripple of C_1 and C_2 are
$\Delta V_{c1} = 6.1298*10^{-4}$V and $\Delta V_{c2} = 2.7964*10^{-4}$V

I. Conduction Losses

The conduction losses of switched capacitor cells occurred during charging process of the capacitor. When switch S_{ai} is turned OFF, the capacitor C_i (i = 1, 2.....N) is charged to ($V_{dc} - 2V_f$) through two forward biased diodes shown in figure 3, where V_f is the forward voltage drop of a diode. For seven level inverter circuits two similar charging paths operated in parallel with a common switch of S_b. The conduction losses during charging of Capacitor C_i are given by the equation (21)

$$P_{con} = \frac{f_s}{2}\sum_{i=1}^{p} C_i\left(V_f + \Delta V_{Ci}\right)\Delta V_{Ci} \quad (21)$$

Where, p is the number of capacitor charging parallel path
p, i = 1, 2.....N
f_s is the switching frequency
N is the number of SC cell

Large capacitance reduces the voltage ripple, thereby reduces the power loss.

For 100mF capacitor and 1kHz switching frequency, conduction loss can be calculated as

$P_{con} = 0.03573W$

J. Switching Losses

Switching losses occur during turning ON and turning OFF time and they dominate for the fast switching operations. When the switch is turned OFF, its voltage increases from 0 to maximum voltage. The switching loss P_{sw} of the switch during one switching cycle is given by the equation (22)

$$P_{sw} = f_s C_{ds} V_s^{\,2} \quad (22)$$

Where, f_s is the switching frequency
C_{ds} is the parasitic capacitance of MOSFET
V_s is the voltage across the switch

For any full bridge inverter switch, V_s = 12.6V, C_{ds} = 440PF and 1kHz switching frequency

$P_{sw} = 6.98544*10^{-6}$ W

V. PULSE WIDTH MODULATION SCHEMES

To control and to generate high quality output waveform, an appropriate modulation scheme is required. Among the various modulation schemes, an important family of modulation technique, multicarrier pulse width modulation stands out because it offers significant simplicity and easy to implement switching waveforms.

For the Simulation Sinusoidal Alternative Phase Opposition Disposition (APOD) PWM technique is used, because APOD shows the minimum THD for all switching frequency [9].

The frequency ratio m_f is defined in the relation (23)

$$m_f = \frac{f_c}{f_m} \quad (23)$$

where, f_c is the carrier (triangular) signal frequency
f_m is the modulating signal frequency

Carrier frequency or switching frequency is chosen as 1kHz for the optimum THD and modulating signal frequency as 50Hz. ie., $m_f = 20$.

The amplitude modulation index m_a is defined as

$$m_a = \frac{2A_m}{(m-1)\,A_c} \quad (24)$$

where, A_m is the amplitude of the modulating signal
A_c is the peak amplitude of the carrier signal

For an m-level inverter, (m-1) carriers with same carrier frequency f_c and same peak-to-peak amplitude A_c are continuously compared with the sinusoidal reference waveform having amplitude A_m and reference frequency f_m.

In Sinusoidal Alternative Phase Opposition Disposition (APOD) alternate carriers are phase shifted by 180˚ from its neighbour [6] - [9] as shown in figure 8.

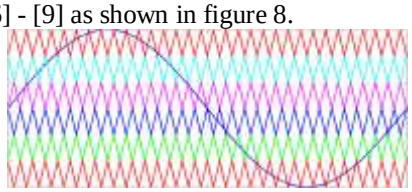

Fig. 8. Sinusoidal Phase Disposition PWM

VI. SIMULATION AND RESULTS

For an input of 5V, switching frequency f_c as 1kHz and reference frequency f_m as 50Hz, the proposed multilevel inverter was simulated in Matlab Ra2014a. The capacitance C_i can be determined properly with considering the voltage ripple of the capacitors C_i.

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A. Gate Pulse Generation

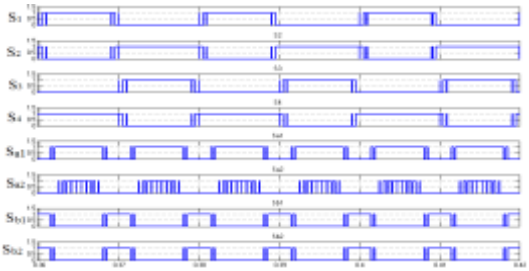

Fig. 9. Switching Pulses using APOD techniques

Gate signals are obtained by comparing modulating signal at fundamental frequency (50Hz) with triangular carrier signal which are at 1kHz frequency. Figure 9 shows the seven switching pulses using APOD technique.

B. Input current

Figure 10 shows the input current drawn by the circuit. Input current which is a combination of diode currents and switch current during the capacitor discharging period. Diode current is used to charge the capacitors when the switch S_{ai} is turned OFF. Maximum input current drawn from the input source is 0.45A.

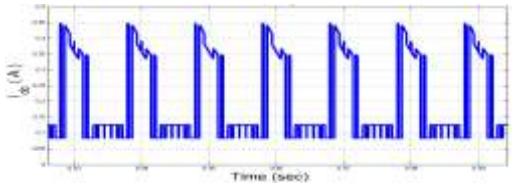

Fig. 10. Input Current

C. Diode current

Figure 11 shows the current through the diodes. The maximum current is 0.45A during the charging period of capacitor, because capacitor is charged through input source, diodes D_i and common switch S_{bi}. Current through diode D_1 can be calculated by deducting the switch Sa1 current from the input current.

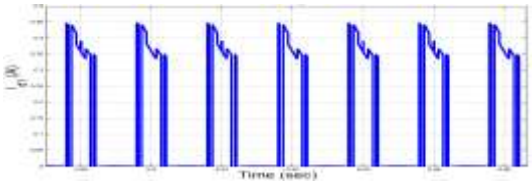

Fig. 11. Current through Diode D_1

D. Diode Voltage

Figure 12 shows the voltage across the diode D_1. Diode D_1 experiences 0.8V forward drop and -4.2V reverse voltage.

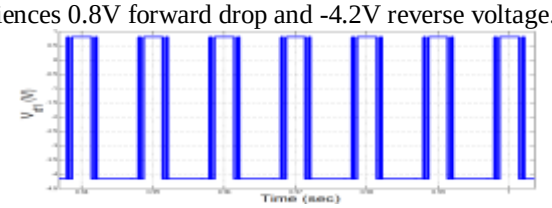

Fig. 12. Voltage across Diode D_1

Figure 13 shows the voltage across the diode D_2. From the waveform forward diode drop is 0.8V and -3.4V reverse voltage.

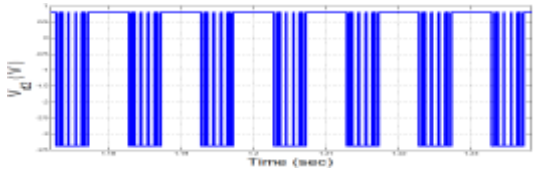

Fig. 13. Voltage across Diode D_2

E. Capacitor Voltage

During S_{ai} turned OFF, capacitor C_1 starts charging to a voltage equal to (V_{dc} - V_f) through forward biased diode D_1. In this work, V_{dc}= 5V and Forward diode drop, V_f = 0.8V means capacitor charged to 42V as shown in figure 15.

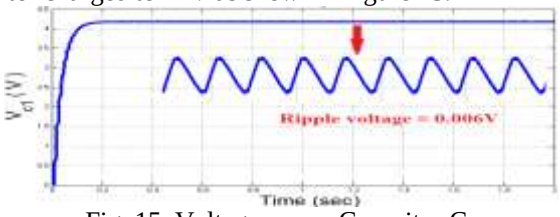

Fig. 15. Voltage across Capacitor C_1

Capacitance ripple voltage from the simulation for C_1 is 0.006V. The capacitor to be used should be such that it should retain the voltage specified. Figure 16 shows the voltage of capacitor C_2. Here capacitor C_2 charges through two forward biased diodes. So C_2 charged to a voltage equals to (V_{dc} - 2V_f) = 3.4V. From simulation voltage ripple of capacitor is 0.0032V.

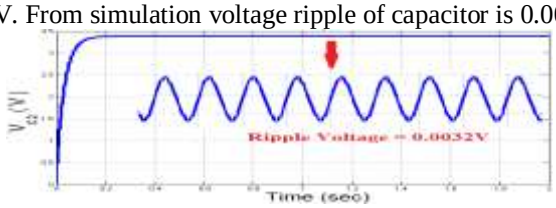

Fig. 16. Voltage across Capacitor C_2

F. Voltage Stress Across the Switches

Figure 14 shows the voltage stress using APOD PWM technique. From the simulation, voltage drop across the switches in the full bridge inverter is 12.6V. Voltage stress across switch S_{a1} and S_{b1} is 5V, for S_{a2} is 4.2V and maximum stress across switch S_{b2} is 9.2V.

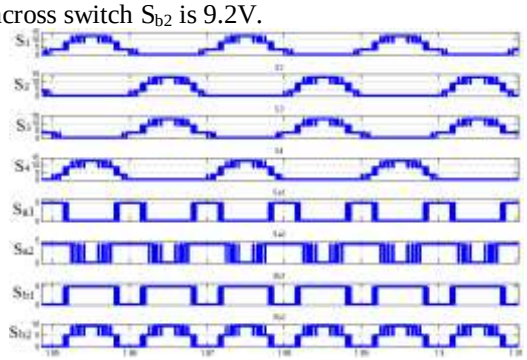

Fig. 14. Voltage Stress of Switches

G. OutputVoltage and output current (R LOAD)

. Figure 17 show the seven level output voltage using Alternative Phase Opposition Disposition PWM technique.

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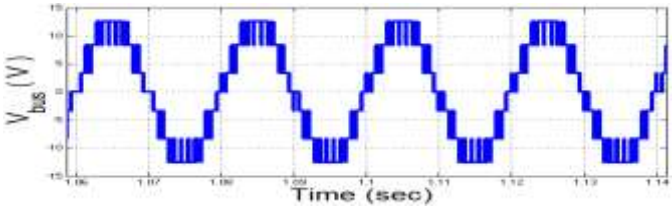

Fig. 17. Output Voltage (R Load)

Figure 18 shows the Seven level output current of the inverter using 100Ω load resistance.

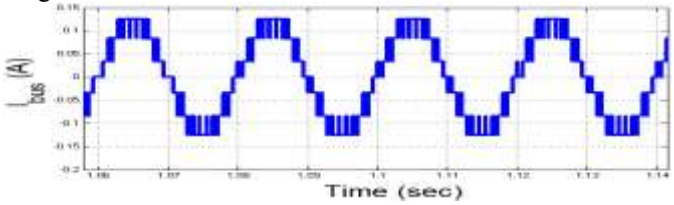

Fig. 18. Output Current (R Load)

H. FFT Spectrum

Figure 19 shows the FFT spectrum of output voltage using the Alternative Phase Opposition Disposition technique with a modulation index m_a = 1. Here %THD is calculated by considering 30 cycles of output voltage with a fundamental frequency of 50Hz.

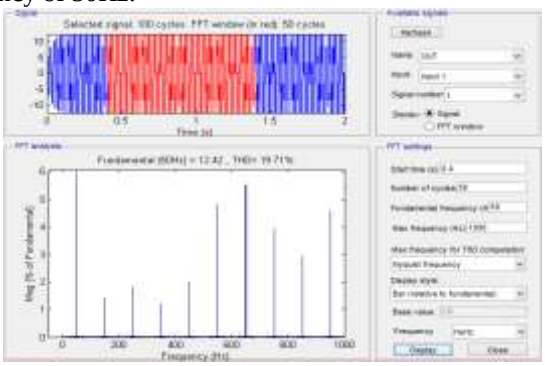

Fig. 19. FFT Spectrum Output Voltage

I. Filter Circuit

A typical capacitor input filter consists of a filter or reservoir capacitor C_1, connected across the rectifier output, an inductor L, in series and another filter or smoothing capacitor, C_2, connected across the load, R. Assuming C_1=C_2=C,

$$\text{Capacitor, } C = \frac{1}{4\pi^2 L f_c^2} \quad (31)$$

$$\text{Cut-off frequency, } f_c = \frac{1}{2\pi\sqrt{LC}} \quad (32)$$

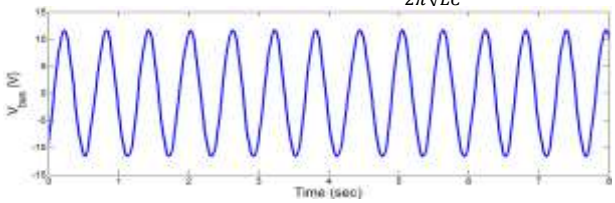

Fig. 20. Filter Output Voltage

Figure 20 shows the output voltage of the inverter using filter.

VII. VARIABLE FREQUENCY DRIVES

A. Power Grid Applications

Basically, a typical GCPV system consists of PV array, maximum power point tracker (MPPT) unit(s) or DC-DC converter, inverter and utility grid. The produced DC power is then converted into AC power using inverter before delivered into the utility grid. This inverter is acts as boosted DC-AC converter. So the input DC required to generate the grid voltage is less compared to other multilevel configuration and number of series connected module in the PV array can also be reduced. The three phase structure for a switched capacitor multilevel inverter can be implemented by combining three individual inverter blocks for each phase connected together. As the number of level in the output increases input DC required is reduces. Thus the size of entire system minimized because boost converter design can be eliminated. Eleven level three phase inverter output voltage is shown in figure 21.

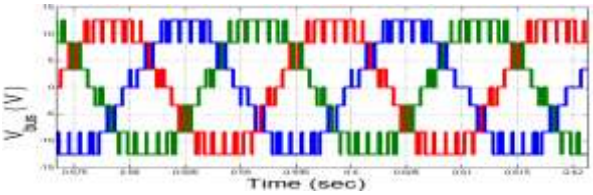

Fig. 21. Three Phase Output Voltage

B. Variable Frequency Drives

Modified Three Phase Series/Parallel Switched Capacitor Topology is applied to the Induction machine Drive. Here by varying the modulating signal frequency, this inverter can be used for Variable Frequency Drives [20].

Machine Parameters

Ratings of Three Phase Induction Motor:

Voltage (line-line) = 460 V
Frequency f = *50 Hz*
Nominal power of motor P_o= *7.5 kW*
Rated speed N_r = *1440 rpm*
Rated current I = *2.650 A*
Load torque T_l = *47.5 N-m*
No. of poles P = *4*

Parameters of Three Phase Induction Motor:

Stator Resistance R_s = *0.6* Ω
Stator leakage Inductance L_{ls}= *4.5 mH*
Rotor Resistance R_r= *0.7* Ω
Rotor leakage Inductance L_{lr} = *4.5 mH*
Mutual Inductance L_m = *80 mH*
Moment of Inertia J = *0.1 kg-m2*

1. **Modulating Signal Frequency f_m = 50Hz**

Fig. 22 shows the Electromagnetic Torque applied to induction machine Drive. Simulation is carried out for a zero reference electromagnetic torque.

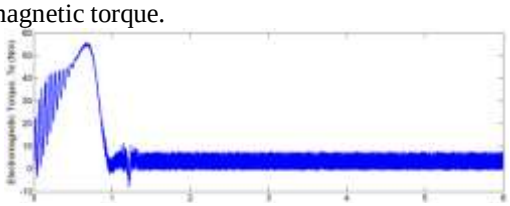

Fig. 22. Rotor Torque

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Fig. 23 shows the Rotor speed of the induction machine Drive. From the simulation result we can say that the induction motor drive nearly catches the rotor speed and we can get the desired speed variation. Although there are changes in speed, the actual torque of the motor is almost near to the reference torque. There are some distortions in actual torque at the point where speed is drastically changing.

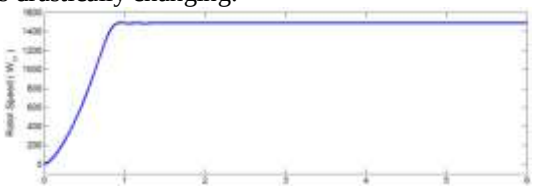

Fig. 23. Speed

Fig. 24 shows the Stator Current in each phase of the induction machine Drive, which are almost near to sinusoidal and having lesser distortion.

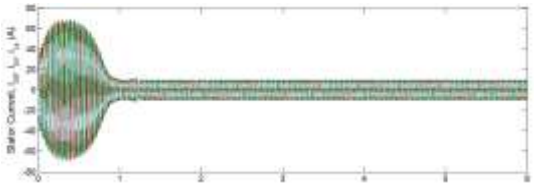

Fig. 24. Stator Current

2. Modulating Signal Frequency f_m = 60Hz

Fig.25 shows the Electromagnetic Torque applied to induction machine Drive.

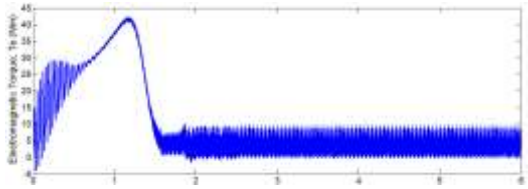

Fig. 25. Rotor Torque

Fig.26 shows the Rotor speed of the induction machine Drive.

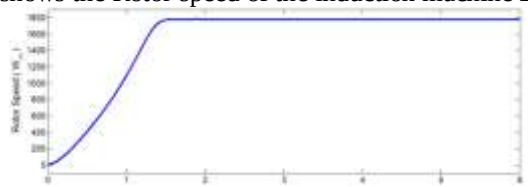

Fig. 26. Speed

Fig.27 shows the Stator of the induction machine Drive.

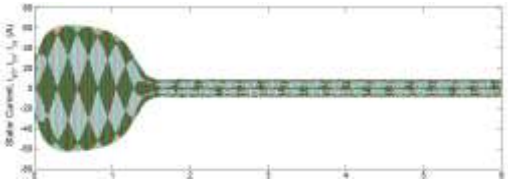

Fig. 27. Stator Current

As the frequency of the modulating signal varies motor performance varies, time at which reference torque occurs varies.

VIII. CONCLUSIONS

In this paper, a switched capacitor boost multilevel inverter with reduced number of switches was developed and it was simulated in MATLAB/Simulink software. Alternative Phase Opposition Disposition PWM with a reference signal of 50 Hz and carrier of 1.6 kHz were used to generate gate pulses. Gate pulses generated are verified according to the switching pattern in simulation result. A multilevel output is simulated with a higher voltage by using only a small input voltage and it was determined that as the number of levels increases in the output, the input required to generate a particular output decreases considerably. At each level the voltage increases that is it doubles triples etc per level. Also it was seen by FFT analysis that % THD value decreases with increase in level. The total harmonic distortion was seen to be reduced to 19.78% for seven level output with 12.6 V as amplitude for an input of 5V. By varying the modulating signal frequency, this inverter can be used for Power Grid Applications and Variable Frequency Drives.

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