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FPGA IMPLEMENTATION OF FIR FILTER ARCHITECTURE BASED ON FIXED WIDTH BOOTH MULTIPLIER WITH SIGN-DIGIT BASED CONDITIONAL PROBABILITY ESTIMATION

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Abstract— **Digital Filters are intensively used in all DSP sub-systems and they are said to be the most important component of any DSP applications. Therefore large number of research has been carried out on designing such filters. Reduced power consumption and area optimization are the most important considerations that have to be taken care of while designing filters. Adders, Flip-Flops and Multipliers are the major blocks of Finite Impulse Response (FIR) Filter, Where multiplier is the major part and the performance of Filter depends on it. In this Paper fixed width booth multiplier with sign-digit-based conditional probability estimation is used in filter architecture. Booth-encoded Sign-digit-based Conditional Probability Estimation (BSCP) multiplier optimizes the area and power consumption by reducing the partial products and using compensation circuits. The proposed FIR filter architecture is designed using Verilog HDL and synthesis is done in Xilinx ISE Design tool, simulation results are verified in Modelsim and implemented on FPGA Spartan 3 XC3S200TQ144-4 device.**

Keywords— **FIR Filter, Modified Booth Encoding, BSCP Multiplier, Impulse Response, FPGA**

I. INTRODUCTION

Digital signal processors have their applications in various fields like audio, video, speech and image processing applications.

Filters are the basic structures for DSP applications, recent advancements in VLSI technology made it possible to design filter architecture with minimum operations [1]. Based on the impulse response digital filters are of two types Finite Impulse Response (FIR) Filter and Infinite Impulse Response (IIR) filter. The multiplier structure in these Filter are more power and area consuming devices. Compared to IIR Filter FIR Filter has advantageous in terms of computation efficiency and its stability thereby reduces the number of arithmetic computations [2]. The drawbacks of FIR filter are, at the time of implementation it requires more number of arithmetic operations and thereby reduces the speed of execution and requires larger area and power [4]. The basic arithmetic operation in FIR Filter is Multiplication and it occupies the major hardware components such as area, delay and power consumption. Therefore it is important to minimize these parameters to reduce the arithmetic operations performed by multiplier. Parallel processing and Block processing considered with its frequency spectrum characteristics and short convolutions can be used to achieve low power and low area filter architecture [11]. Modern digital communication systems and wireless sensor networks use such power efficient filters in their applications.

In the proposed work existing Multiplier structure is replaced with Booth Encoded Sign-digit based Conditional Probability estimation (BSCP) multiplier. 4-tap FIR Filter architecture includes adders, multipliers and D Flip-Flops. BSCP multiplier minimizes the number of arithmetic computations in multiplication. It is performed as two step operations first with the help of booth encoding it produces the partial products and then using compensation circuit they are minimized. Next these products are added using adder circuit to produce final product.

II. EXISTING METHODOLOGY

A. Finite Impulse Response Filter –

Filters are used to remove the unwanted or distorted signals. Filtering means applying various mathematical operations on the signal to reduce the distortion and enhance the signal strength.

FIR Filter is a digital filter that has finite impulse response, where the present and past non-recursive inputs varies the

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output of the filter hence it does not require any feedback structure. The transfer function of FIR Filter is expressed as-

$$H(Z)=\frac{Y(Z)}{X(Z)}=\sum_{n=0}^{N-1} h(n).Z^{-n} \qquad (1)$$

Where X(Z) is the input samples and Y(Z) is the output samples of the filter. In the above equation h(n) represents the filter response.

Some of the terms used in FIR Filter are Impulse Response, it is the set of co-efficient. Tap is a co-efficient/delay pair that indicates the quantity of memory required and number of calculations during implementation of filter and its performance of filtering. Increasing number of tap means more stop band attenuation, less ripple, narrow filters etc,. Multiply Accumulate unit (MAC) for amplification of the corresponding co-efficient to collect the sample data and delay elements.

B. BSCP Multiplier –

Fixed width multipliers have wide range of applications in energy efficient digital signal processing systems. In designing the filter architecture multiplier is the structure that requires more computations and produces maximum delay, so it is necessary to reduce the area and increase the speed of operation of multiplier. Few such effective and efficient multiplier architectures are

- Post truncated multiplier where product is obtained after complete calculations where results are accurate but requires larger area and hardware components.
- Direct truncated multiplier directly removes the least significant bit without computation and hence its accuracy rate is very low.

BSCP is also one such method used to reduce the partial products with retaining the accuracy of the multiplier. It uses modified Booth algorithm which is used for high speed multiplications, in this the computation time of the algorithm it can reduce half number of partial products.

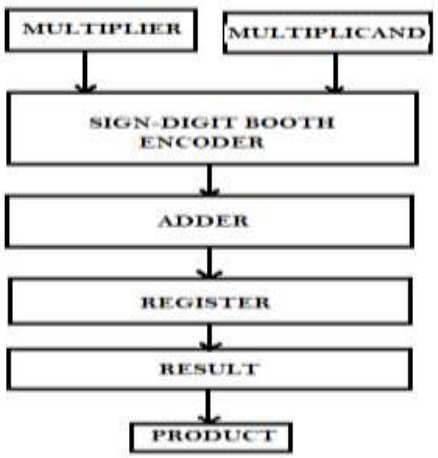

Fig. 1. Structure of BSCP Multiplier

Modified Booth Encoding (MBE) also known as Radix-4 encoding technique it is used to increase the speed and reduce the area of the multiplier circuit, multiplication is performed by repeated addition operations. In BSCP a lower mean square error can be obtained which reduces the computation accuracy. In partial product generator product terms are obtained by multiplying one bit of multiplicand with one bit of multiplier if there is more number of bits in the operands. It reduces the redundancy of the circuit and also speeds the process of multiplication.

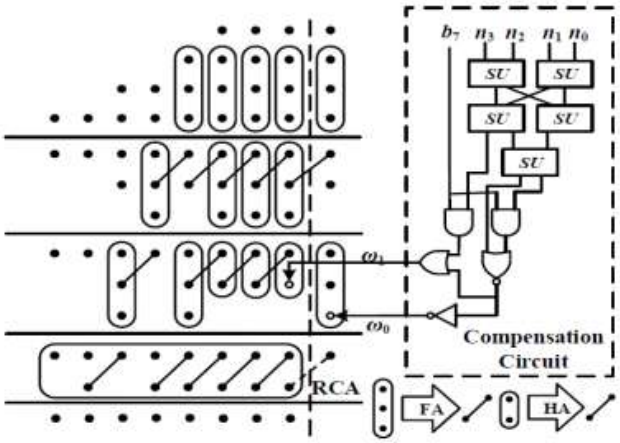

Fig. 2. Circuit Structure of BSCP Multiplier

In the above Fig. 2. we can see the circuit structure of BSCP multiplier, where the partial products in truncation part are reduced using compensation circuit which is the combination of sorting network and Multiplexer unit. Multiplexer unit is used for estimation of the value that is further added with partial product major part. This compensation circuit reduces area in larger value and hence the power consumption also reduces.

III. PROPOSED SYSTEM

Digital Filter accepts digital input and produces digital output, Filter function is to block specific range of frequency and passing the original signal to the output. Multipliers, adders and delay elements are the basic building blocks of Filter. In the FIR filter architecture existing multiplier structure is replaced by the BSCP multiplier which reduces the area and power consumption

For a N tap FIR Filter it requires N filter coefficients, (N-1) delay elements and (N-1) adder blocks. For a 4-Tap Filter architecture design it requires 3 delay elements and 3 adder blocks. The design of 4-Tap FIR Filter is shown in the Fig. 3. Let N be the order of the filter, whereas the number of coefficients required to design the FIR filter is N+1. Where x(n) represents the input, D represents the delay samples and

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h(n) represent the coefficients that are multiplied with the input sample.

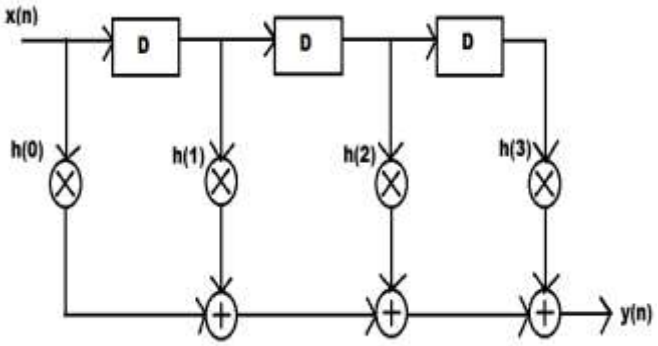

Fig. 3. Structure of 4-Tap FIR Filter with BSCP Multiplier

In this paper a 4 tap conventional FIR filter is designed, verilog-HDL is used for coding and to check the functional correctness synthesis is done using Xilinx ISE and simulation is done using Modelsim and it is implemented on Spartan-3 device. Area utilized for the design and its power consumption are observed.

IV. FPGA IMPLEMENTATION

FPGA Spartan-3 XC3S200TQ44-4 device is used to implement the proposed FIR Filter design, Sparten-3 provides powerful development platform for all the designs and supports easily implementation of all designs.

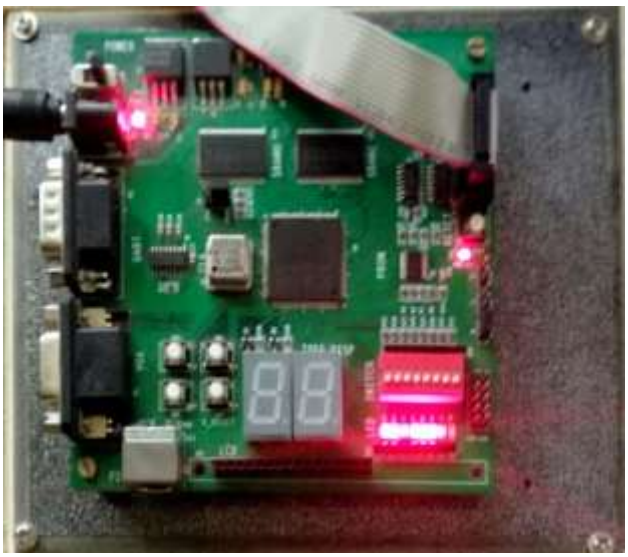

Fig. 4. Implementation of FIR Filter design on FPGA

Fig.4 shows the output for the given set of input conditions. Inputs are given by switches and outputs are observed on the LED.

V. RESULT AND ANALYSIS

Filter architecture with existing booth multiplier and proposed BSCP multiplier are compared. The comparison results obtained shows that the proposed filter design with BSCP multiplier is more efficient compared to existing design. Fig 5 shows the simulation waveforms for proposed filter design with BSCP multiplier.

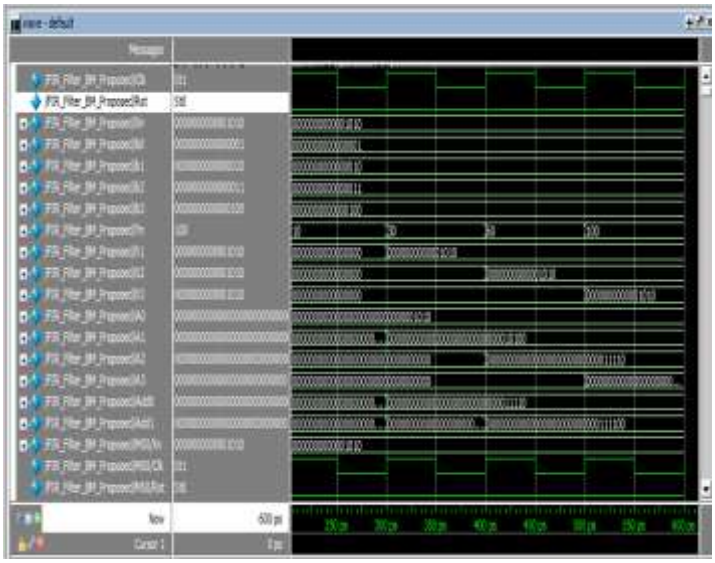

Fig. 5. Simulation Waveform of Proposed System using Modelsim

Table -1 Device Utilization Summary of Existing System

Device Utilization Summary			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Flip Flops	48	55,296	1%
Number of 4 input LUTs	3,796	55,296	6%
Logic Distribution			
Number of occupied Slices	2,068	27,648	7%
Number of Slices containing only related logic	2,068	2,068	100%
Number of Slices containing unrelated logic	0	2,068	0%
Total Number of 4 input LUTs	3,892	55,296	7%
Number used as logic	3,796		
Number used as a route-thru	96		
Number of bonded IOBs	114	633	18%
IOB Flip Flops	32		
Number of GCLKs	1	8	12%
Total equivalent gate count for design	34,313		
Additional JTAG gate count for IOBs	5,472		

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Power summary:	I(mA)	P(mW)
Total estimated power consumption:		743
Vccint 1.20V:	505	605
Vccaux 2.50V:	55	138
Vcco25 2.50V:	0	0
Clocks:	260	312
Inputs:	50	60
Logic:	29	35
Outputs:		
Vcco25	0	0
Signals:	48	58
Quiescent Vccint 1.20V:	118	141
Quiescent Vccaux 2.50V:	55	138

Fig. 6. Power Consumption Report for Existing System

Table -2 Device Utilization Summary of Proposed System

Device Utilization Summary			
Logic Utilization	Used	Available	Utilization
Number of Slice Flip Flops	47	55,296	1%
Number of 4 input LUTs	3,193	55,296	5%
Logic Distribution			
Number of occupied Slices	1,802	27,648	6%
Number of Slices containing only related logic	1,802	1,802	100%
Number of Slices containing unrelated logic	0	1,802	0%
Total Number of 4 input LUTs	3,225	55,296	5%
Number used as logic	3,193		
Number used as a route-thru	32		
Number of bonded IOBs	114	633	18%
IOB Flip Flops	31		
Number of GCLKs	1	8	12%
Total equivalent gate count for design	26,889		
Additional JTAG gate count for IOBs	5,472		

Power summary:	I(mA)	P(mW)
Total estimated power consumption:		265
Vccint 1.20V:	106	127
Vccaux 2.50V:	55	138
Vcco25 2.50V:	0	0
Clocks:	0	0
Inputs:	0	0
Logic:	0	0
Outputs:		
Vcco25	0	0
Signals:	0	0
Quiescent Vccint 1.20V:	106	127
Quiescent Vccaux 2.50V:	55	138

Fig. 7. Power Consumption Report for Proposed System

Table -3 Area, power and delay comparison

Method Name	Area in Number of LUT			Power (mw)	Delay (ns)
Spartan-3 3S4000IFG900 -4	LUT	Slices	Gate count		
FIR with existing system	3796	2068	34313	743	76.677
FIR with Proposed system	3193	1802	26889	265	100.87

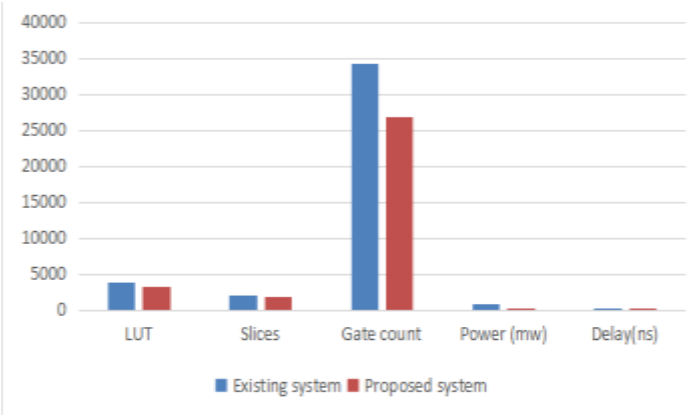

Fig. 8. Comparison between Existing and proposed system

Table 1 and 2 show the device utilization summary of existing and proposed system where the number of LUTs, Slices and gate count of proposed system is reduced. In Fig 6 and 7 we can observe the power consumption of both the designs respectively, where the power required for proposed system is 265mw and existing system requires 743mw of power. Table 3 shows the comparison results of area, power and delay obtained from Xilinx software for both the systems. In figure 8 comparison results are shown using graph. By observing these results it is clear that the proposed FIR filter architecture is more efficient than existing system.

VI. CONCLUSION

FIR filters which are used in various applications are designed using VLSI technology with so many advancements. Study on FIR filter shows that the computational blocks of the filter are adders, multipliers and Flip-Flops, where the multiplier is the block that requires more area and power. In this work BSCP multiplier is used for filter design which is more efficient and faster. Design is implemented on Spartan-3 device and the simulation results shows that use of BSCP multiplier in FIR filter design reduce both area and power. Hence it is concluded that the designed filter requires less chip area and reduced power consumption.

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