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COMPARATIVE STUDY OF DIFFERENTIAL BOOST INVERTERS

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Abstract— **Output voltage of traditional full bridge inverter is less than input DC voltage. In applications when input voltage is low, the front end step up converter is usually required presenting a two stage power conversion. Dual boost inverter (DBI) can realize single stage conversion, which has the advantages of simple structure, less power devices and boost ability. The traditional modulation strategy of DBI makes all power switches operate in high frequency and sustain high voltage or current stress, which leads to heavy conduction and switching loss. So the Half Cycle Modulation (HCM) strategy can be used, which makes power switches work in high frequency just in half cycle, and can reduce the switching and conduction losses power devices greatly. Furthermore, to reduce the current circulation loss in DBI, an improved DBI with two clamping switches is can be used based on HCM, which can bypass the inductor current with low stress switches, therefore the loss caused by circulation current can be greatly reduced. The simulation of a dual boost inverter with half cycle modulation technique has been used to find out the losses and the boosting of the output. The simulations are done by using MATLAB/SIMULINK software. DBI prototype has been implemented in the lab. The advantages of the HCM strategy and improved DBI with two clamping switches are verified using experimental results.**

Keywords— **Differential Boost Inverter, Half Cycle Modulation, clamping switches, efficiency**

I. INTRODUCTION

Full-bridge inverter is the mostly used topology to realized DC-AC power conversion. It can be seen as Buck inverter and the output AC voltage is always lower than input DC voltage. In applications when the input voltage is low, an additional front-end DC-DC converter is required to realize voltage step-up conversion. The two-stage structure is complex in system structure and controller design and the efficiency is also influenced by two stages.

Although line frequency transformer can be utilized to step up the input voltage, it will be voluminous. In order to minimize the power components, many single-stage inverters were introduced [1], which is beneficial to the improvement of power density and efficiency due to its simple structure and less power device. Z-source inverter which can be viewed as a quasi-single-stage inverter takes the advantage of the passive network to boost voltage and allows shoot through situation in bridge legs [2], [8]. But the drawbacks of high Z-source capacitor voltage stress and huge inrush surge may influence the efficiency, and vast passive components will also go against integration. So a novel active buck-boost inverter can be used [9], which can boost the voltage, performs buck and boost conversion in a quasi-single-stage inverter. But this single-stage inverter has too many power switches.

So that leads to the introduction of the Dual Boost inverter (DBI) based on two symmetrical bidirectional boost DC-DC converters [1]. The DBI consists of two boost converters whose outputs are out-of-phase sinusoidal voltages with the same DC bias. The output voltage can be higher than the DC input voltage [10] based on the step-up characteristic of Boost converter. To mitigate low-frequency ripple current, a waveform control was presented. A dynamic linearizing Modulator based Boost inverter was introduced to improve its power bandwidth. Traditional modulation method makes each group of the bidirectional boost DC/DC converters produce the sinusoidal AC voltage with same DC bias [4], [6-7]. However, all power switches of the converter operate in high frequency under this modulation, and the power switches sustain high voltage/current stress, which leads to a heavy conduction and switching loss. Meanwhile, a circulation current will flow through the inductors and which will be against the improvement of efficiency due to the additional losses caused by this current.

So, the half cycle modulation (HCM) strategy has been introduced [5], which makes two boost groups operate by turns, each group output a half-steamed bread wave voltage with a DC bias. The output side can get a pure sinusoidal AC voltage output by differing the two outputs. HCM can reduce the number of power switches working in high frequency, and reduce the stress of the switches and inductors. The switching and conduction loss of switches can be greatly reduced, and also the core loss and copper loss of inductors can be reduced. Furthermore, to reduce the current circulation loss in DBI, an improved DBI with

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two clamping switches is introduced based on HCM. The improved topology can achieve higher efficiency with low stress clamping switches operating in half cycle and line frequency.

II. PROPOSED TOPOLOGY

A. **Traditional and half cycle modulation strategies –**

Fig.2 shows the key waveforms under traditional modulation strategy. The output of the Boost converters is sinusoidal AC voltage with same DC bias.

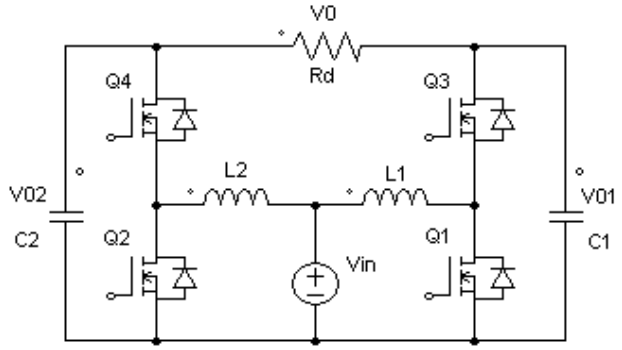

Fig. 1. Differential Boost inverter circuit diagram

The operational principle of the DBI converter under traditional modulation strategy is given as following. Four power switches are all working in high frequency as shown in Fig.1. Defining V_{01}, V_{02} as voltage of C_1, C_2, V_{dc} as offset voltage, V_{in} is input DC voltage, V_m is magnitude of output AC voltage, d_1, d_2 is the duty cycle of Q_1,Q_2. Through the appropriate control logic, V_{01}, V_{02} can be obtained as follows:

$$V_{01}(t) = V_{dc} + (½)V_m\sin(\omega t)$$

$$V_{02}(t) = V_{dc} + (½)V_m\sin(\omega t-\pi)$$

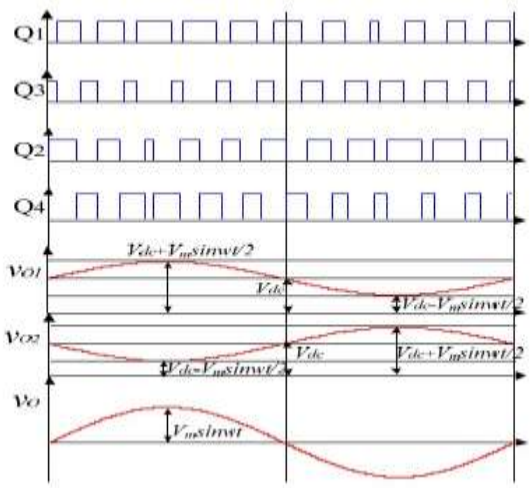

Fig. 2. Traditional modulation strategies and key waveforms

$$V_0(t) = V_{01}(t) - V_{02}(t) = (V_{in}/1\text{-}d_1(t)) – (V_{in}/1\text{-}d_2(t))$$

$$V_0(t) = V_{01}(t) - V_{02}(t) = V_m\sin(\omega t)$$

Where, $V_{dc} \geq V_{in}+V_m/2$

The waveforms of V_{01}, V_{02} and V_o are shown in Fig 2, the voltage of V_{01}, V_{02} is sinusoidal with a DC bias. The output voltage V_o is sinusoidal by differing the V_{01}, V_{02}. In the positive period of the output voltage, switches Q_1, Q_3 worked in high frequency, which is complementary with each other, Q_2 is turned off, Q_4 is turned on, the output voltage of capacitance C_1 can be obtained as above equation, the voltage of C_2 is V_{in}. In the negative period of the output voltage, switches Q_2, Q_4 worked in high frequency, which is complementary with each other, Q_1 is turned off, Q_3 is turned on, the output voltage of capacitance C_2 can be obtained as equation2, the voltage of C_1 is V_{in}.

In a switching cycle, the converter under HCM has 4 switching modes. Fig. 3 shows the control strategy of HCM, and Fig.4 gives the equivalent circuits of the switching modes in the switching cycle. Before analysis, some assumptions are given: 1) all the switches and diodes are ideal; 2) all the capacitors and inductance are ideal; 3) C_1=C_2, L_1=L_2.

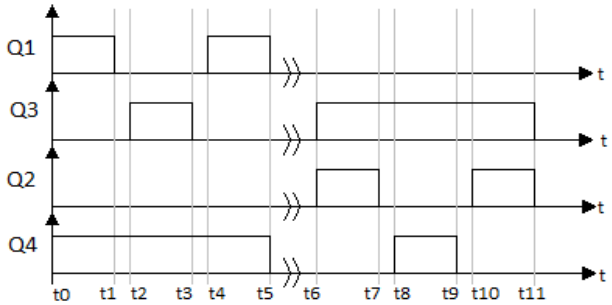

Fig. 3. Control strategy under half cycle modulation.

B. **Modes of operation** –

In the period that output voltage is positive

1) Mode 1 [t_0, t_1]: At t_0, Q_1, Q_4 is turned on, the input voltage is applied on L_1, and the input current charges L_1. Load current i_o will flow through Q_4 (D_4) to V_{in}, which supplied by C_1, as shown in Fig 4(a).

2) Mode 2 [t_1, t_2]: The period is dead time, at t_1, Q_1, Q_2, Q_3 are turned off, Q_4 is turned on, the current i_{L1} flow through D_3 or D_1 (according to the current direction), as shown in Fig. 4(b). Load current i_o will flow through Q_4 (D_4) to V_{in}.

3) Mode 3 [t_2, t_3]: At t_2, Q_3 is turned on, i_{L1} flow through Q_3 (D_3). Load current i_o flow through Q_4 (D_4) to V_{in}. The current flow path is shown in Fig 4(c).

4) Mode 4 [t_3, t_4]: The period is also dead time, and the operating mode is the same as the mode 2.

In the period that output voltage is negative:

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5) Mode 5 [t_6, t_7]: At t_6, Q_2, Q_3 are turned on, the input voltage is applied on L_2, and the input current charges L_2. Load current i_o will flow through Q_3 (D_3) to V_{in}, which supplied by C_2, as shown in Fig 4(d).

6) Mode 6 [t_7, t_8]: The period is dead time, at t_7, Q_1, Q_2, Q_4 are turned off, Q_3 is turned on, the current i_{L2} flow through

D_4 or D_2 (according to the current direction), as shown in Fig. 4(e). Load current i_o will flow through Q_3 (D_3) to V_{in}.

7) Mode 7 [t_8, t_9]: At t_8, Q_4 is turned on, i_{L2} flow through Q_4 (D_4). Load current i_o flow through Q_3 (D_3) to V_{in}. The current-flow path is shown in Fig 4(f).

8) Mode 8 [t_9, t_{10}]: The period is also dead time, and the operating mode is the same as the mode 6.

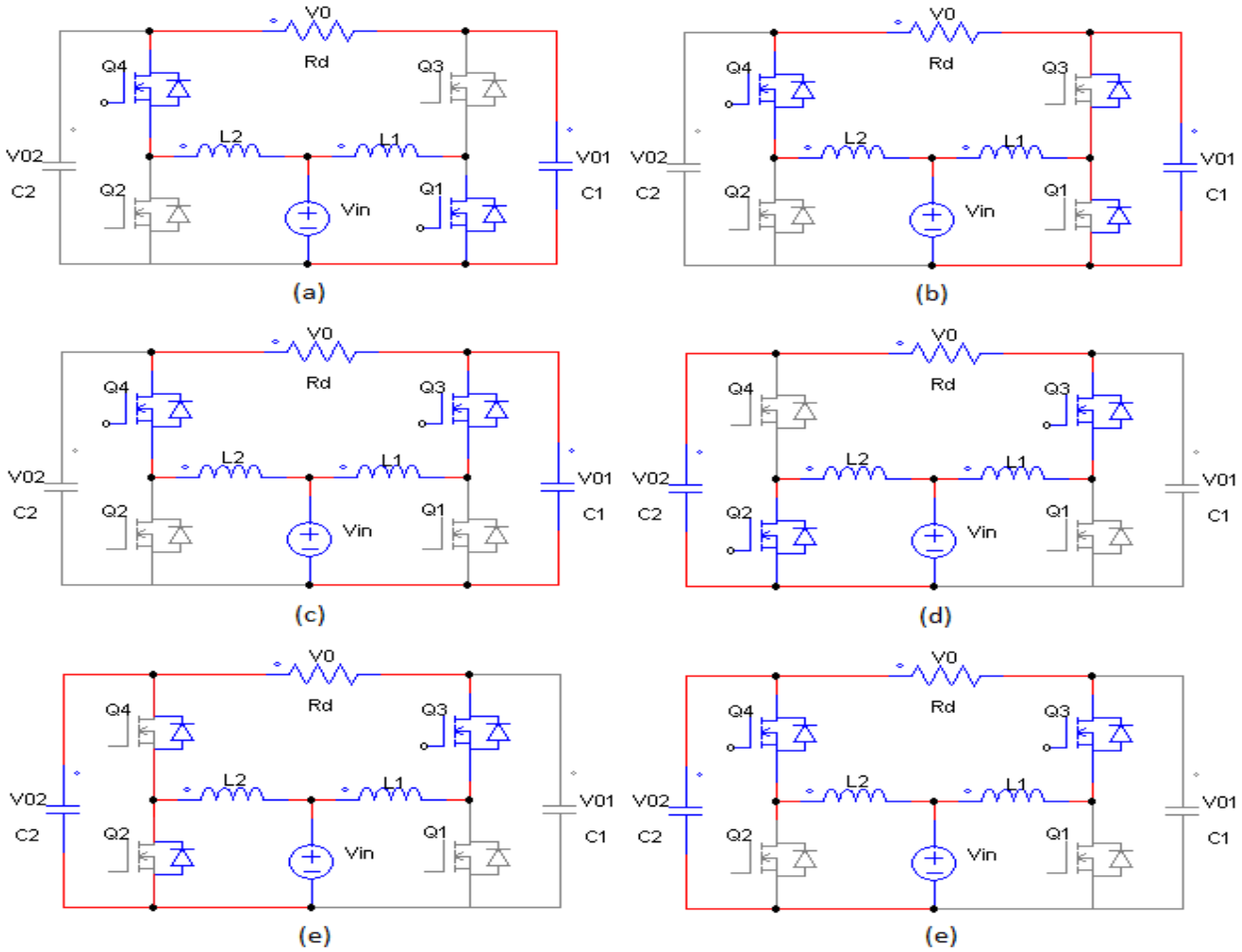

Fig. 4. Equivalent circuits of switching modes. (a) [t_0,t_1],(b) [t_1,t_2] or [t_3,t_4],(c) [t_2,t_3],(d) [t_6,t_7],(e)[t_7,t_8] or [t_9,t_{10}] and [t_{10},t_{11}]

C Improved DBI with two clamping switches

Whether traditional modulation method or HCM strategy are utilized, current circulation of the converter still exists, which means the core loss and copper loss of inductors L_1, L_2 will exist all the time. In half line cycle, there is only one inductor need to play a booster role under half cycle modulation strategy, the other output side can be clamping to V_{in} by using a clamping switch. The clamping switches operate in line frequency, and the voltage stress is much lower. For low voltage stress applications, low cost MOSFET can be utilized which means the conduction loss is lower than IGBT in the same condition, therefore low cost MOSFET can be applied. The topology is shown in Fig.5 shows the modulation strategy and the key waveforms.

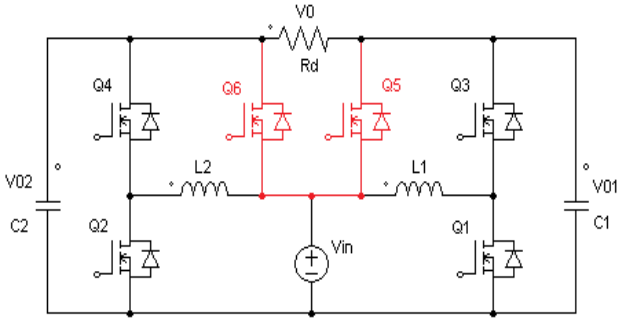

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Fig. 5. Improved main circuit with clamping switches

The converter with clamping switches mode is the same as the mode under HCM. The voltage/current stress is the same as HCM, except clamping switches. The current stress of clamping switch is i_o, the voltage stress of clamping switch is ($V_o - V_{in}$), which is lower than both of TM and HCM. The clamping switches obviously have a further lower voltage stress, leading a lower conduction loss. Moreover, clamping switches reduce the inductor core loss and copper loss generated by circulation current.

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III. SIMULATION MODEL AND RESULTS

The details of the parameters are showing in Table 1.

Table-1 Simulation parameters used for simulation.

Parameter	Symbol	Value
Input Voltage	V_{in}	**80V**
Output Voltage	V_o	**110V**
Rated Capacity	P_o	**500VA**
Fundamental Frequency	F_o	**50Hz**
Switching frequency	F_{sw}	**20KHz**
Inductance	L_1,L_2	**500µH**
Capacitance	C_1,C_2	**20µF**

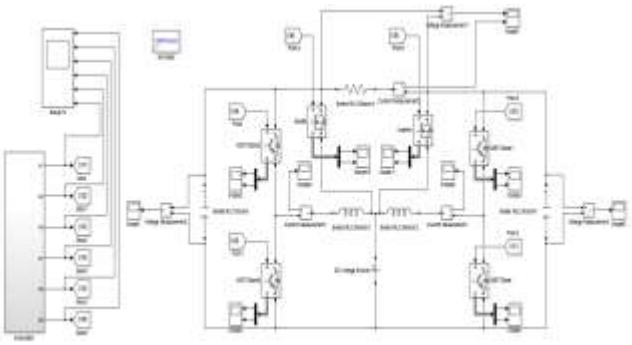

Fig. 6. Simulink model of improved DBI with clamping switches.

Fig. 6 shows the SIMULINK model of the improved dual boost inverter with two clamping switches.

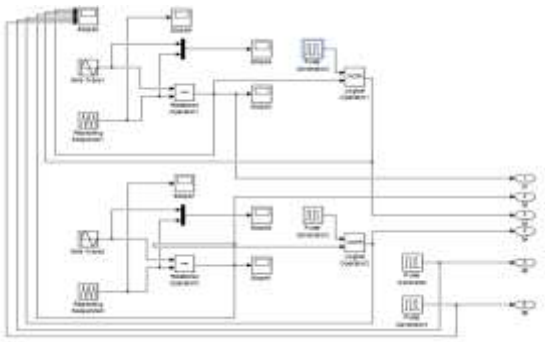

Fig. 7. Control strategy of switches.

Fig.7 shows the control strategy of the switches which is the half cycle modulation technique.

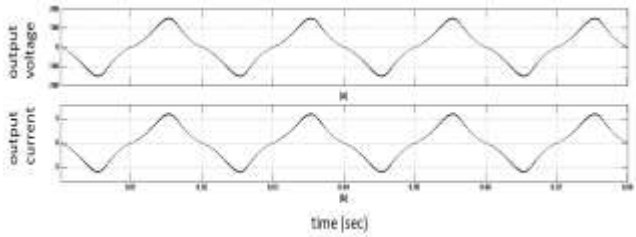

Fig. 8. Output waveforms (a) output voltage (b) output current.

The output voltage across the load is the differential voltages across the capacitors. So the output voltage that occurs across load is an AC voltage. Since the load is a resistive load the output current will be in phase with output voltage. The output voltage will be a boosted voltage than the input voltage. For the input voltage of 80V the output obtaining is 110V (rms) and the output power obtained is 500W.

IV. EXPERIMENT AND RESULT

Experimental set up of the dual output DC-DC converter in Fig. 1 is done. To obtain the switching pulse micro controller Arduino Mega 2560 is used. The program for control pulse is written in C language. The program is verified and the frequency is checked by simulating the program using Proteus software. The output of the micro controller is given to a driver IC TLP250. These pulses are fed to the gate of switches in the power circuit.

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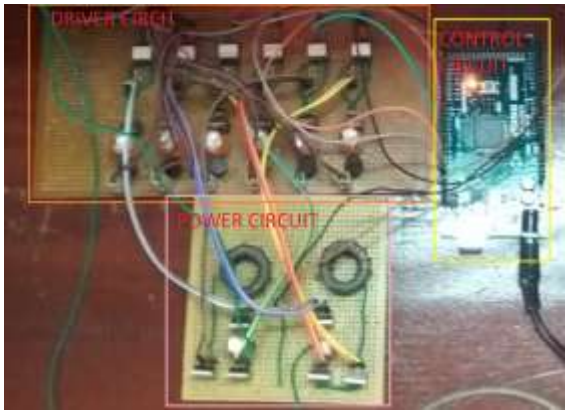

Fig. 9. Dual Buck Full Bridge Inverter

The Switching pulses of the high frequency switches are generated by using PWM pins and Timers of Arduino. These are shown in Fig and Fig is that pulses for the high frequency switches Q1, Q2, Q3 and Q4. These are SPWM controlled switches. The Switching pulses of the bridge switches are generated by using digital pins of Arduino. Fig. 10 and Fig. 11 shows these pulses. The proposed scheme is tested using ordinarily image processing. From the simulation of the experiment results, we can draw to the conclusion that this method is robust to many kinds of watermark images.

In the prototype the source voltage is 10 V. The output of the differential boost inverter is shown in Fig. 13. It is in power frequency 50 Hz. Since it is a boost inverter the maximum voltage in the output is greater than the input. The bridge input is given to the high frequency switch which is controlled by SPWM. Fig. 10 and Fig. 11 indicate that Q_1, Q_3 are working in high frequency, Q_2, Q_4 are turned off, Q_6 is turned on, which will reduce core loss and copper loss of inductance because of the current circulation in the period that output voltage is positive. Q_2, Q_4 are working in high frequency, Q_1, Q_3 are turned off, Q_5 is turned on in the period that output voltage is negative. The clamping switches sustained a further lower voltage stress, which can reduce the conduction loss further. In the prototype, it works on 50Hz frequency.

Fig. 10. Gate pulses of Switches (a) Q1 and Q2

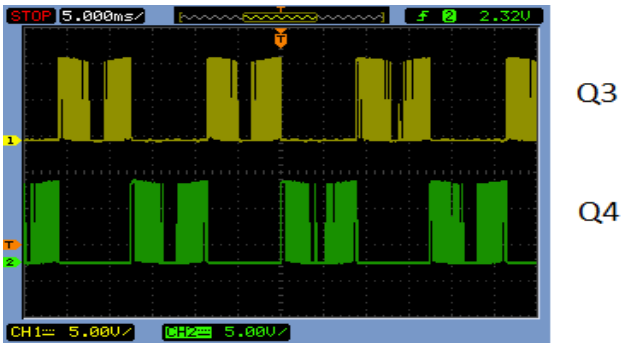

Fig. 11. Gate pulses of Switches (a) Q3 and Q4

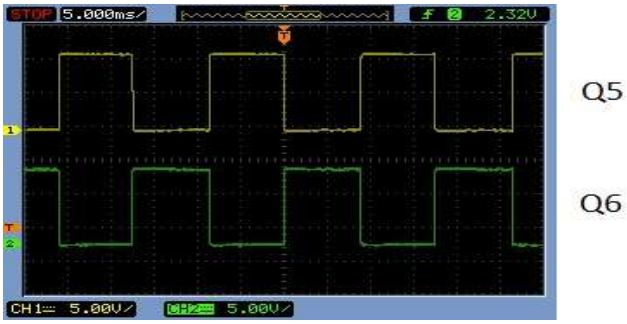

Fig. 12. Gate pulses of Switches Q5 and Q6

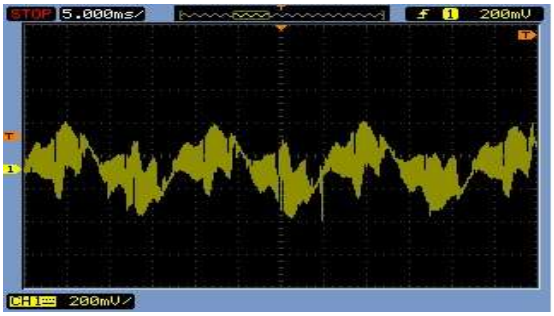

Fig. 13. Output Voltage Vo

A comparative study has been made between differential boost inverters and improved differential boost inverter with two clamping switches. Different comparisons have been made. That is the variations in THD for different load resistances, variations in THD for different switching frequencies and variation in efficiencies for different output powers have been compared. For lower resistances the THD of the DBI will be less than that of improved DBI. The THD tends to increase for increase in load resistances for DBI. But for improved DBI the THD will decrease for low resistance values and that will remain almost constant for increase in the load resistance. The THD of the DBI will become more than that of improved DBI for higher load resistances. The variations in THD for different switching frequencies will be almost same for DBI and improved DBI. For lower values of switching frequencies, the THD will be more and

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that will tend to decrease and will become steady for increase in frequency.

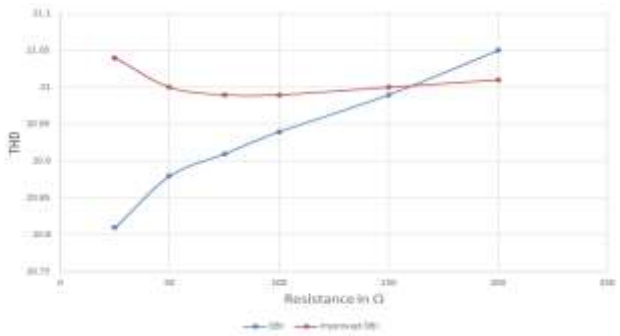

Fig. 14. Comparison between DBI and Improved DBI for Different Load Resistance

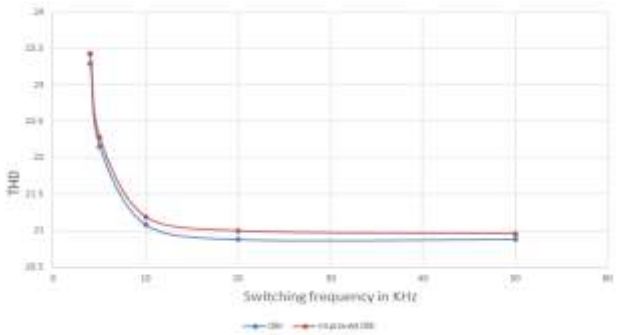

Fig. 15. Comparison between DBI and Improved DBI for Different frequencies

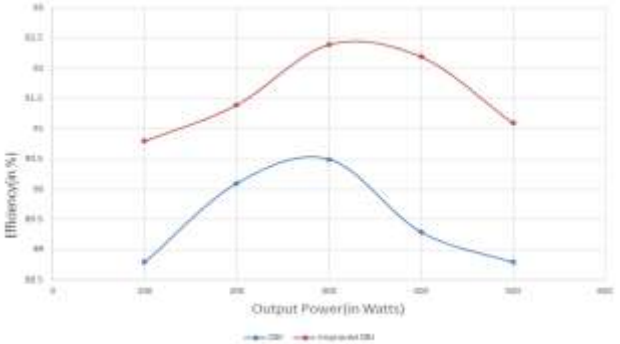

Fig. 16. Measured Efficiency of DBI and Improved DBI

The efficiency of the improved DBI will be greater than that of the DBI. The efficiency curve tends to increase for increase in the output power and it will start to decrease after some value of output power as shown in Fig. 16. From Fig. 16 it is clear that the efficiency is maximum at an output power of 325W and the maximum efficiency of improved DBI is 92.4. For DBI maximum efficiency is 90.5 at an output power of 280W.

IV. CONCLUSION

An improved DBI under half cycle modulation with clamping switches has been designed. According to the analysis and simulation results, the half cycle modulation strategy with clamping switches of DBI keeps the advantage of buck-boost ability. Furthermore, it brings the following advantages over the DBI with traditional PWM techniques: Only half of the switches are working in high frequency under HCM compared with T-M, which obviously reduces the switching loss of the DBI, the voltage/current stress of the switches is lower with HCM than T-M, which will further reduce the switching loss and conduction loss of the power switches, the inductor current is lower with HCM, which also reduce the magnetic loss and clamping switches is helpful to low the current circulation loss of inductor and IGBT. With low stress MOSFET, it can also reduce the conduction loss of circulation current. The reduction in the losses means the efficiency of DBI can be improved with HCM because high frequency switches is less than traditional modulation, also the inductor current stress is lower; in addition, the improved DBI can further improve the efficiency because of the low conduction loss by introducing low stress switches. The theoretical analysis and simulation results have been given to verify the analysis. The analysis results are verified using the experimental setup and thus improvements are obtained.

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