International Journal of Engineering Applied Sciences and Technology, 2017
Vol. 2, Issue 5, ISSN No. 2455-2143, Pages 160-166
Published Online March-April 2017 in IJEAST (http://www.ijeast.com)

INTERLEAVED BUCK CONVERTER WITH SYNCHRONOUS RECTIFICATION

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***Abstract*— A modified Interleaved Buck Converter (IBC) with continuous input current, extremely low output current ripple, low switching losses and improved step-down conversion ratio is presented in this work. The implemented converter used for synchronous rectification. In this converter, diode is replaced by switch to reduce losses. For this converter, 180 degree phase shifted pulses and its complementary pulses are required. Circuit is simulated with 200V DC input voltage and 24V DC output voltage is verified.**

Keywords— **Two Phase Interleaved Buck Converter, Continuous Conduction Mode, CIBC, NIBC, MIBC**

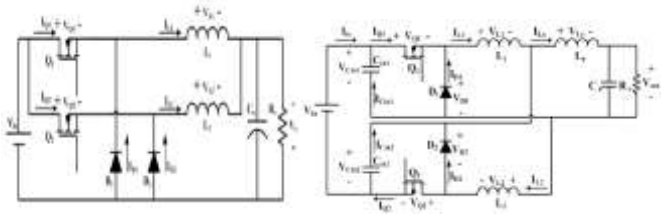
I. INTRODUCTION

One of the most popular converters for the consumer electronic industry is the DC-DC step-down converter, also known as the buck converter. The synchronous buck converter is straightforward in concept, and is used heavily in consumer electronics. A synchronous buck converter produces a regulated voltage that is lower than its input voltage, and can deliver high currents while minimizing power loss. The new interleaved buck converter has many advantages except power loss in a diodes are high. To reduce power losses, we introduce a synchronous buck converter technique in which diodes are replaced by switches. These switches are operated by complementary pulses of other two switches. By doing this, new interleaved buck converter gets converted into synchronous buck topology. The advantage of using the synchronous buck topology is that it reduces power loss taking place in diode during conduction period which is equal to the product of the forward voltage drop and the current flowing during conduction period.

The rest of the paper is organized as follows. Proposed circuit and modes of operation are explained in section II. Simulation models and results explained in section III. Experimental results are presented in section IV. Concluding remarks are given in section V.

II. INTERLEAVED BUCK CONVERTERS

The Fig. 1. (a) shows conventional interleaved buck converter and Fig. 1. (b) is new interleaved buck converter. Conventional IBC problem in high input voltage applications is that the voltage stress of all switches is equal to the input voltage. Due to high voltage stress of switches and diodes, Conventional IBC has high switching losses.



(a) (b)

Fig. 1. (a) Conventional (b) New Interleaved Buck Converter

New IBC which suitable for high input voltage, high step-down, non-isolated applications with low output current and continuous input current. But this converter also having power loss. It is similar to a three level buck converter, but the two input capacitors are not connected to each other and also there is an auxiliary inductor at the converter output stage. The two active switches are controlled by two PWM pulses 180 degrees out of phase.

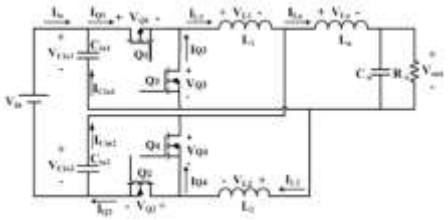


Fig. 2. Modified Interleaved Buck Converter

Synchronous buck converter technique in which instead of diode as shown in Fig. 2. Switches has been used which

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complementary operates with its corresponding switch Q_3 which in turn is complementary with Q_1 and similarly Q_4 is complementary with Q_2. New interleaved buck converter gets converted into synchronous buck topology.

The advantage of using the synchronous buck topology is that it reduces power loss taking place in diode during conduction period which is equal to the product of the forward voltage drop and the current flowing during conduction period.

A. Modes of Operation –

Interval 1 [t_0–t_1]:

The equivalent circuit of this interval is shown in Fig. 3. Prior to this interval switches Q_1 and Q_2 are off, the Q_3 and Q_4 are ON and the input capacitors C_{in1} and C_{in2} are charged. At t_0, Q_1 is turned on, so Q_3 turns off. In this interval C_{in2} is charged through V_{in} and L_1, and also C_{in1} is being discharged through L_1-L_o-C_o. In addition, L_1 current is increasing through both of the mentioned current paths. L_2 current is decreasing in this state.

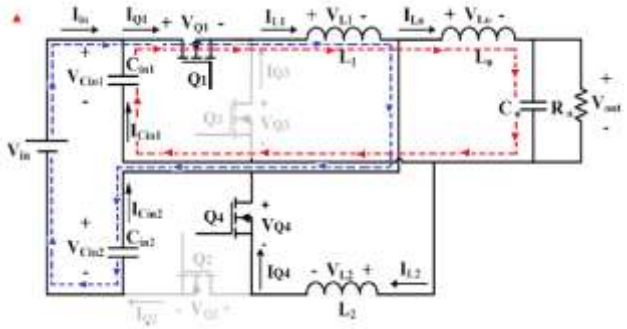

Fig. 3. Equivalent Circuit in Mode

Interval 1 [t_1–t_2]:

The equivalent circuit of this interval is shown in Fig. 4. This interval starts when Q_1 turns off. By turning Q_1 off, L_1 continues it's current and turns Q_3 on. Part of the inductor current which was flowing in C_{in1}-L_1-L_o-C_o, continues its path through D_1-L_1-L_o-C_o, and the other part of L_1 current runs through V_{in}-C_{in1}- Q_3-L_1-C_{in2}. So, during this interval, L_1 and L_2 are discharging and C_{in1} and C_{in2} are charging through V_{in}-C_{in1}-Q_3-L_1-C_{in2} and V_{in}-C_{in1}-L_2-Q_4-C_{in2}.

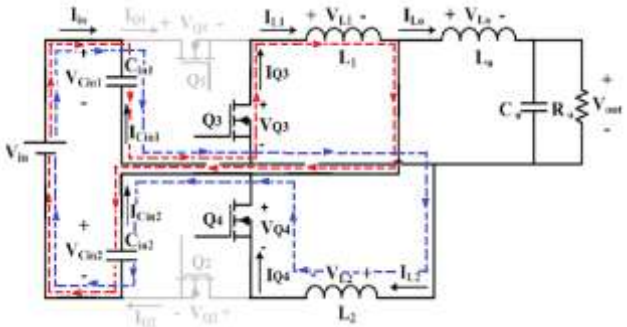

Fig. 4. Equivalent Circuit in Mode 2

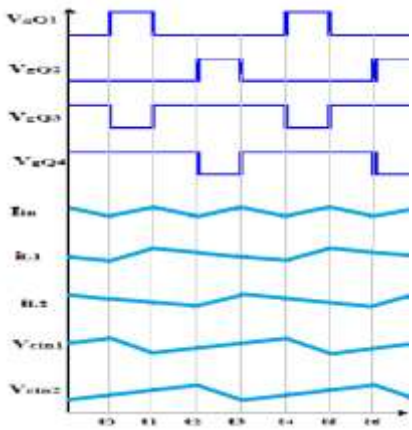

Fig. 5. Theoretical waveform

Due to symmetric operation of two modules in an interleaved converter, the operations of interval 3 and interval 4 are similar to those of interval 1 and interval 2.

III. SIMULATION MODELS AND RESULT

In order to verify the operation principle and the theoretical analysis, conventional, new and modified interleaved buck converters are simulated with MATLAB/SIMULINK simulation software and the simulation parameters are listed in Table 1.

Table 1 – Simulation Parameter

Parameter	Specification
V_{in}	200V
V_{out}	24V
Switching Frequency	100kHz
L_1 & L_2	100µH
L_O	5 µH
Cin1 & Cin2	4.4µF
Co	1 µF

A. Simulink Model:

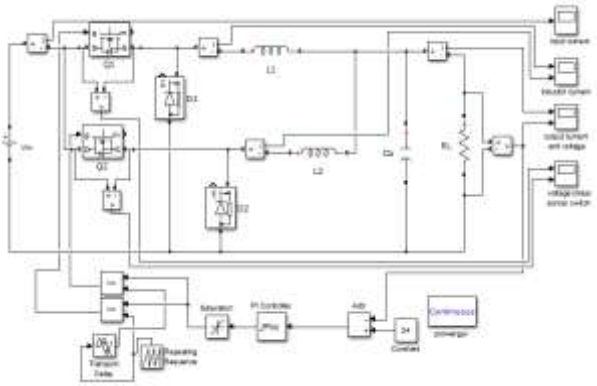

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Fig. 6. Simulink Model of CIBC

Fig. 6. shows that simulink model of conventional interleaved buck converter.

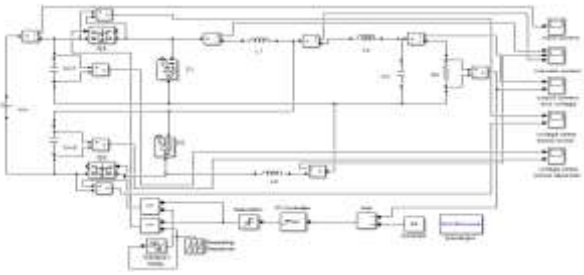


Fig. 7. Simulink Model of NIBC

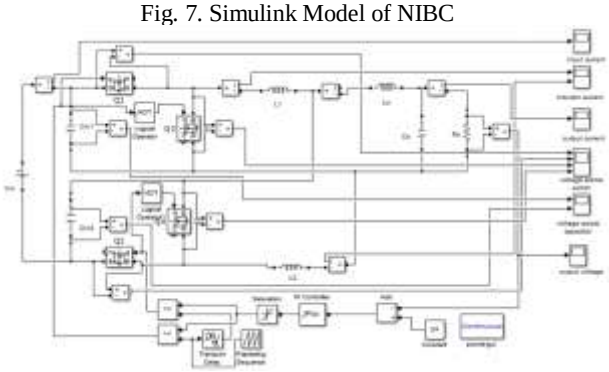
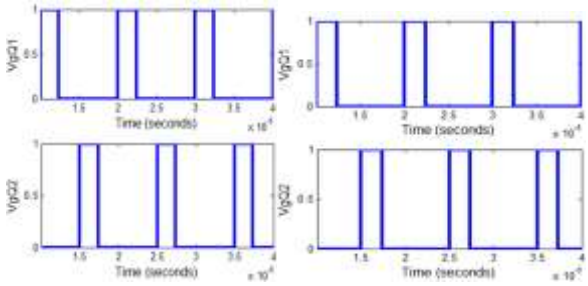


Fig. 8. Simulink Model of MIBC

Fig. 7 and Fig. 8 shows that simulink model of Newinterleaved buck converter and modified interleaved buck converter respectively. Output voltage, output current ripple, stresses across switches and power losses are analyzed from the simulation results.

B. Simulation Result:



(a) (b)

Fig. 9. Switching Pulse (a) CIBC & NIBC (b) MIBC

Fig. 9. (a) shows the switching pulse of CIBC & NIBC and Fig. 9. (b) shows the switching pulse of MIBC. The pulse has amplitude of unity with switching frequency of 100kHz. The first pulse has a phase delay of zero and second pulse is a 180 degree phase shifted.

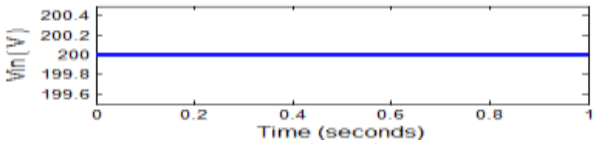
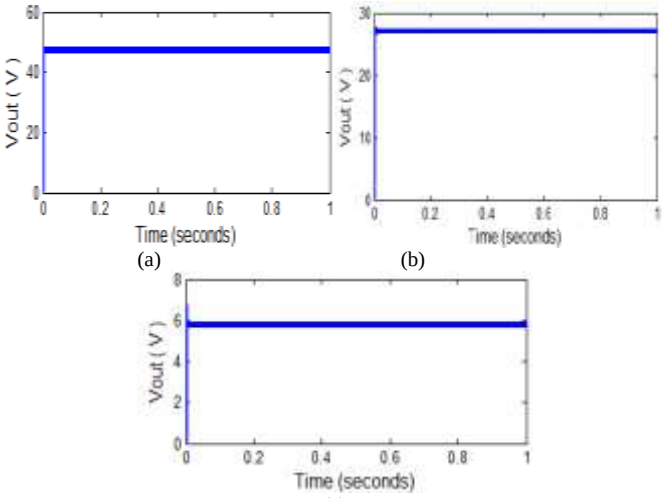


Fig. 10. Input Voltage waveform of CIBC, NIBC and MIBC

Fig. 10 shows the input voltage waveform of CIBC, NIBC and MIBC. Input voltage 200V is given to interleaved buck converters.

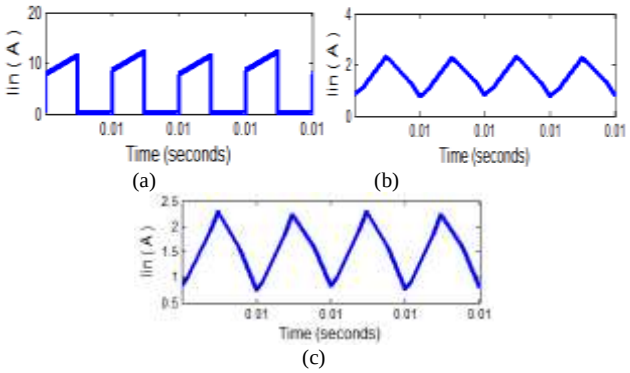


(a) (b)

(c)

Fig. 11. Output Voltage waveform of (a) CIBC (b) NIBC (c) MIBC

Fig. 11 (a), (b), (c) shows the output voltage waveform of CIBC, NIBC and MIBC respectively. For CIBC, output voltage 47.7V DC is obtained. Output voltage 26.5V is obtained in NIBC and for MIBC, 27.15V is obtained.



(a) (b)

(c)

Fig. 12. Input Current waveform of (a) CIBC (b) NIBC (c) MIBC

Fig. 12 (a), (b), (c) shows the input current waveform of CIBC, NIBC, MIBC respectively. For CIBC, input current is discontinuous. Input current for both NIBC and MIBC is continuous.

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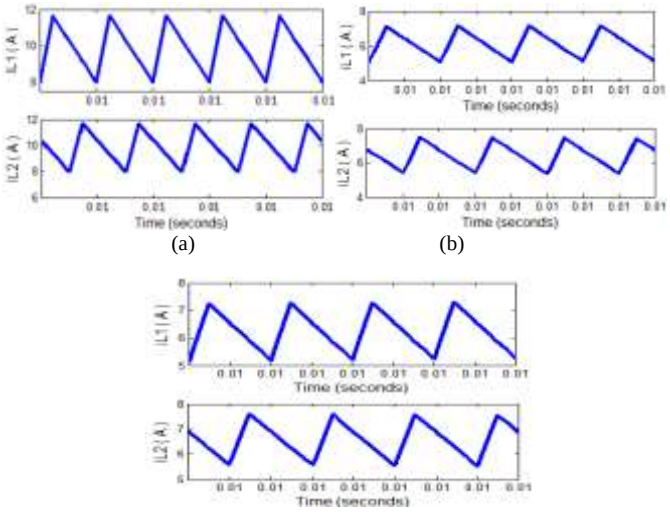
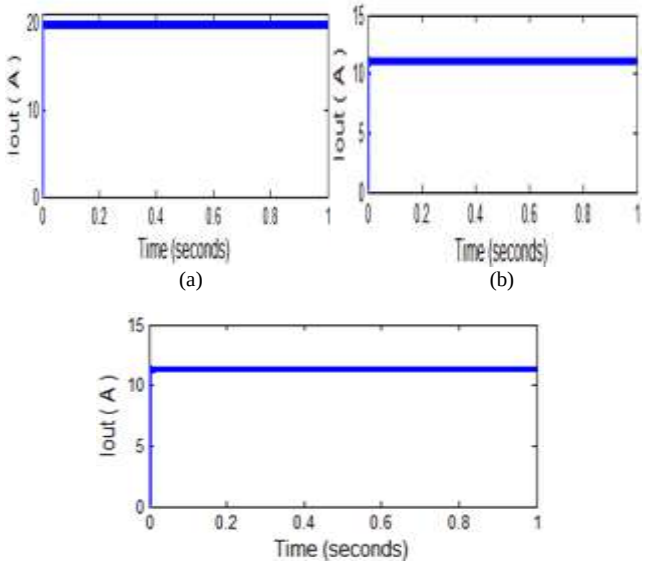


(a) (b)

(C)

Fig. 13. Inductor Current waveforms of (a) CIBC (b) NIBC (c) MIBC

Fig. 13 (a), (b), (c) shows the inductor current waveforms of CIBC, NIBC and MIBC respectively. Inductor current 11.54A is obtained in CIBC. Inductor current 7.25A is obtained in NIBC. In MIBC, 7.4A is obtained.

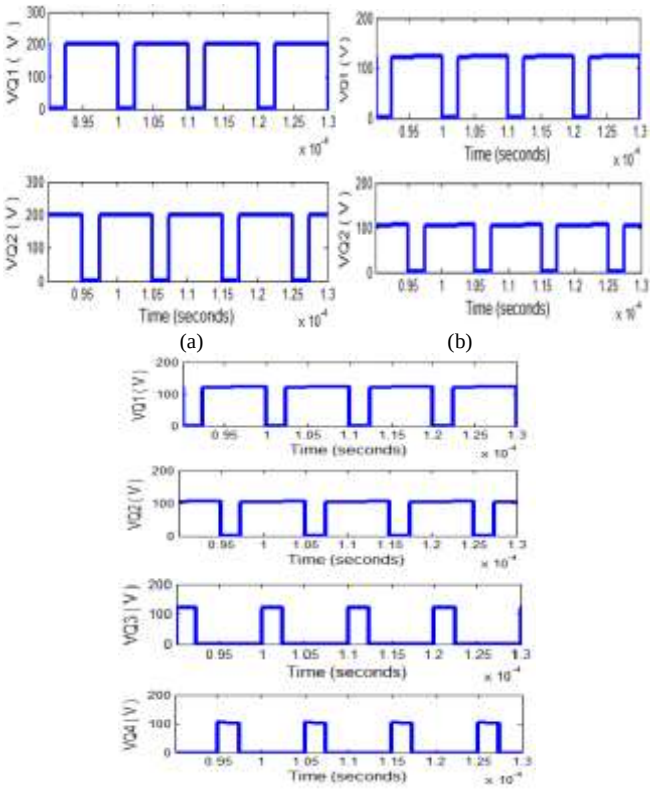


(a) (b)

(C)

Fig. 14. Output Current waveform (a) CIBC (b) NIBC (c) MIBC

Fig. 14 (a), (b), (c) shows the output current waveform of CIBC, NIBC and MIBC respectively. Output current 19.87A DC is obtained in CIBC. Output current 11.04A is obtained in NIBC and in MIBC, 11.31A is obtained.

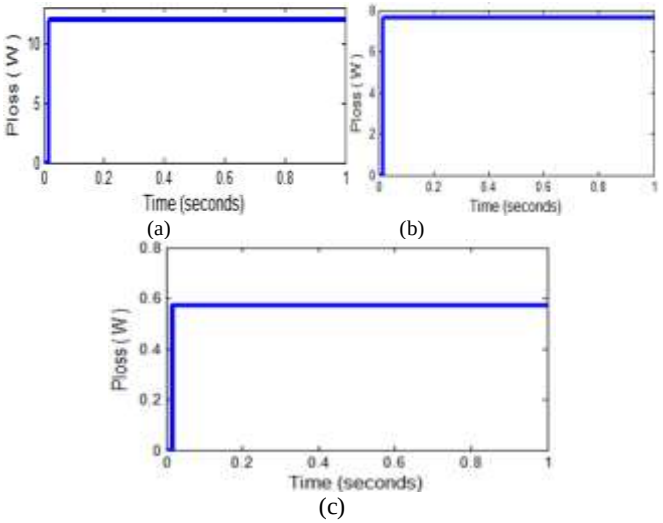


(a) (b)

(c)

Fig. 15. Stress across Switches in (a) CIBC (b) NIBC (c) MIBC

Fig. 15 (a), (b), (c) shows that voltage stress across switches in CIBC, NIBC and MIBC respectively. For conventional IBC, voltage stress across switch 200V is obtained. Voltage stress across switch Q_1 is 125V and Q_2 is 108V is obtained in NIBC. For MIBC, Voltage stress across switch Q_1 and Q_3 is 125V and Q_2 and Q_4 is 108V is obtained.



(a) (b)

(c)

Fig. 16. Power Losses in (a) CIBC (b) NIBC (c) MIBC

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Fig. 16 (a) shows power loss of diode in CIBC. Power loss in diode 12W is obtained. Fig. 16 (b) and Fig. 16 (c) shows that power loss in switches for NIBC and MIBC respectively. Power loss in NIBC is 7.621W is obtained. And power loss in MIBC is 0.56W is obtained.

IV. Experiment and Result

Control circuit and power circuit are implemented in one PCB. Here dsPIC30F2010 is used for generating a pulse and switching frequency. The specification for the hardware is given in Table 2. Hardware is designed for an input voltage of 30V and output voltage of 6V.

Table -2 Prototype Specifications

Parameter	Specification
V_{in}	30V
V_{out}	6V
Switching Frequency	50kHz
L_1 & L_2	220µH
Cin1 & Cin2	3.3 µF
Co	100 µF

A. Experimental Setup:

Fig. 17 shows the final hardware prototype of interleaved buck converter for synchronous rectification. The hardware comprises of control circuit and power circuit. Due to the low switch voltage stress of the proposed converter, four power MOSFETs with a rating of 100V and 22A namely, IRF540 is adopted. L_o is not considered in prototype. In prototype, designed value of output inductor is very small. This small value of inductor does not give any ripple reduction in output current. So, auxiliary inductor is not considered in prototype.

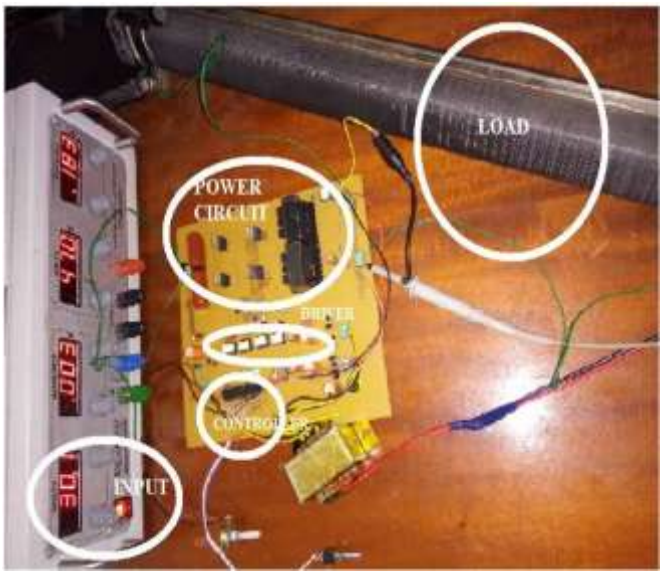
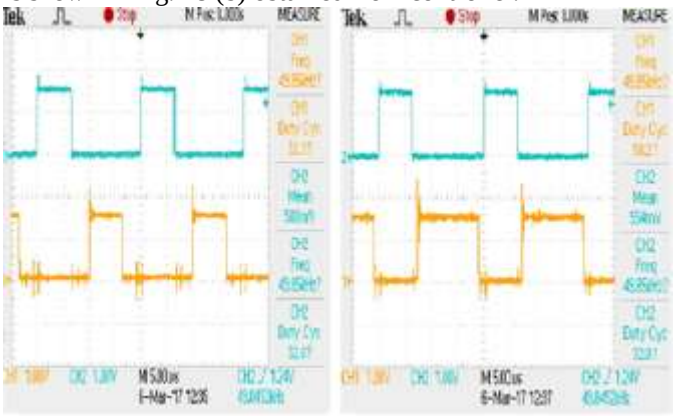


Fig. 17. Experimental Setup

B. Experimental Results:

Fig. 18 shows that switching pulse of modified interleaved buck converter. 180 degree phase shifted pulse for switch Q_1 & Q_2 is shown in Fig. 18 (a) and complementary pulse for Q_3 is shown in Fig. 18 (b) obtained from controller.



(a) (b)

Fig. 18. (a) 180 Degree Pulse and (b) Complementary Pulse

Fig. 19 shows that input and output voltage waveform of proposed converter. Output voltage 6V is obtained from prototype when input voltage 30V is given to modified interleaved buck converter.

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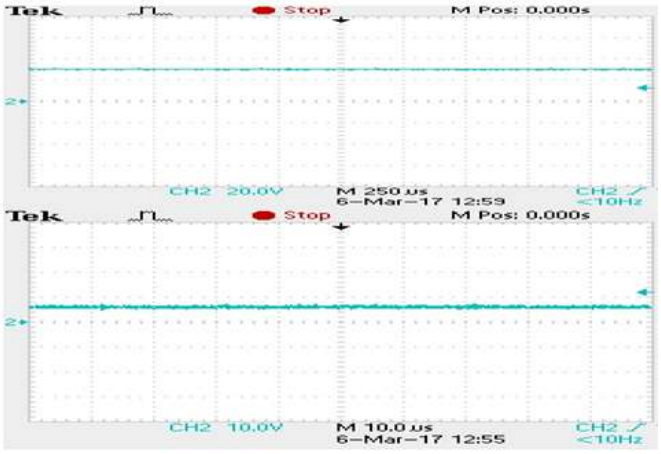

Fig. 19. Input and Output Voltage

V. CONCLUSION

The new interleaved buck converter has many advantages like improved step-down conversion ratio, extremely low output current ripple and low switching losses. Also, the voltage stress of semiconductor components in the new interleaved buck converter and modified interleaved buck converter is much smaller than the conventional interleaved buck converter. Input current is continuous without using any input filter in new interleaved buck converter and modified interleaved buck converter. But in new interleaved buck converter, power loss is much higher. So, we introduce a synchronous buck technology. Two diodes in a new interleaved buck converter are replaced by switches to reduce power loss.

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