*International Journal of Engineering Applied Sciences and Technology,* **2016**
**Vol. 1, Issue 4, ISSN No. 2455-2143, Pages 29-32**
Published Online January-February 2016 in IJEAST (http://www.ijeast.com)

# DOUBLE GATE NMOS STRUCTURE DELINEATED USING $HfO_2$ DIELCETRIC

Divya Punia
Research Scholar,
Department of ECE
NIT Kurukshetra, Kurukshetra

Asha
Teaching Assistant,
Department of ECE
BPSMV, Khanpur Kalan, Sonepat

***Abstract*— Eloquent challenges to circuit design takes place on vigorous scaling contemporary MOSFETs below 100nm. Diminishing dimensions of transistors leads to phenomenon like gate leakage, DIBL, short channel effects. As feature size is reduced by inclusion of interconnect layers, the density of the digital and analog circuit will rise while intrinsic gate switching delay is reduced. This resulted in emergence of DGMOSFET. We have depicted DG NMOSFET with $HfO_2$ dielectric at 35nm scale wielding Silvaco TCAD tool and obtained result. A two dimensional device delineating was carried out and observed that DG NMOSFET with $HfO_2$ dielectric has a low leakage current, subthreshold slope as compared to conventional DG NMOSFET.**

***Keywords*—***DG MOSFET (Double Gate Metal oxide Field Effect Transistor), Short Channel Effect (SCE), TCAD tool, VLSI*

## I. INTRODUCTION

The incessant scaling of semiconductor has sanctioned decrementing the dimensions of contrivance that upgrades the speed of operation and space demand within the VLSI circuits. The short channel effects transpire beyond 45 nm technology [2] which degrades performance of the MOSFETs. Presently there is significant interest in exploring the use of alternative dielectric materials in nano scale regime. By wielding unaccustomed dielectric materials in lieu of silicon reduce series resistance, enhances on current and ameliorate transport properties. The double-gate (DG) MOSFET delineate in Figure one has been contemplated as the most propitious device structure to expand CMOS scaling into the nm regime [1]. The undoped ultra-thin silicon channel is there (i.e., with the background doping concentration of less than 1016 cm-3) to eschew arbitrary dopant placement consequences and mobility degradation cognate to high doping. Sundry modes of operation of DG MOSFET predicated on gate work functions and gate-inequitableness conditions are symmetric (SDG), asymmetric (ADG), or ground-plane (GP) modes. Subthreshold swing (S) and threshold voltage (VT) are hallmark of MOSFET, and their dependences on contrivance parameters are conventionally exploited to benchmark its immunity to short-channel effects (SCE).

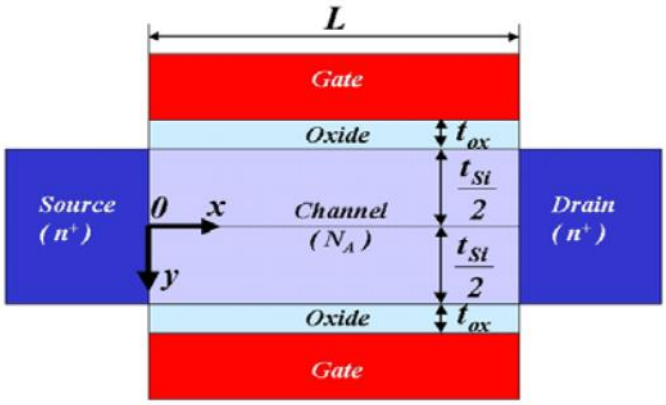


Fig. 1. Cross-section schematic of a DG MOSFET.

DG MOSFET is the portentous device structure in the research field of VLSI. The $SiO_2$ material is customarily taken as a dielectric because of its stability and accessibility in nature. Although $SiO_2$ film approaches it's scaling constraint for its direct tunneling current which makes it more pertinent for low power applications. Subsequently a high k dielectric is much more prudent. Eventually we have chosen $HfO_2$ dielectric material for our research work [4].

## II. DESIGN OF DOUBLE GATE NMOSFET (DG-NMOSFET)

ATHENA and ATLAS device simulator tool of Silvaco TCAD are utilized to delineate and simulate the proposed device.

### A. Device structure and dimensions

Delineating of Double Gate NMOSFET done at gate length Lg of 35nm, gate oxide thickness of 0.00208026 µm, metal gate with work function explicitly set to 4.27eV. Fig.3 predicts designing of DG-NMOSFET by Silvaco TCAD tool. Process

*International Journal of Engineering Applied Sciences and Technology*, 2016
**Vol. 1, Issue 4, ISSN No. 2455-2143, Pages 29-32**
Published Online January-February 2016 in IJEAST (http://www.ijeast.com)

simulation qualifies to extricate some of the design parameters of the simulated double-gate device structure like sheet resistance, channel surface concentration, gate oxide thickness. Table 1 shows the deliberated and perceived parameters (e.g. gate length, gate width, channel length and channel width) for the DG-NMOSFET with $HfO_2$ as gate dielectric.

Table 1: Geometrical parameters of the simulated device design obtained using ATHENA simulation tool.

| PARAMETERS | DG-NMOS with $HfO_2$ |
|---|---|
| CHANNEL CONCENTRATION | 5.06271e+017 atoms/$cm^3$ |
| GATE OXIDE THICKNESS, $t_{ox}$ | 0.00208026 µm |
| GATE LENGTH, $L_G$ | .035 µm |
| GATE WIDTH, $W_G$ | .02 µm |
| CHANNEL LENGTH | .015 µm |
| CHANNEL WIDTH | .485 µm |

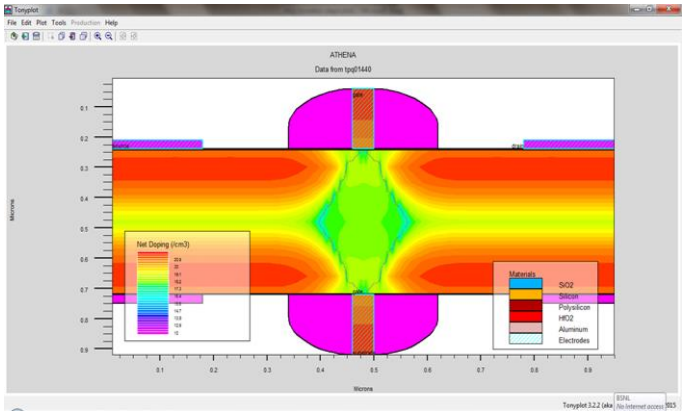


Fig. 2. DGNMOS with $HfO_2$ obtained using ATHENA simulation tool.

### B. Device Simulation

Simulation of DG NMOSFET is done in order to get the output ($I_{DS}$ versus $V_{GS}$ curve) and ($I_{DS}$ versus $V_{DS}$ curve). Besides that, various parameters are extricated such as $V_T$, Sub-threshold, ON current and OFF Current.

### C. $I_{DS}$- $V_{GS}$ CHARACTERISTICS –

To simulate mathematical calculation, by default the program selects model NEWTON and GUMMEL with maximum trap 4. $I_{DS}$ versus $V_{GS}$ characteristics curves are produced by firstly procuring solutions at each step inequitableness points and subsequently solving over the swept partialness variable at each stepped point. $V_{DS}$ values are procured mutually $V_{GS}$ = 1.0 V. After that outputs from these solutions are preserved in .log file. Here drain voltage ($V_{DD}$) is permeating to -0.5 V and gate voltage ($V_{GS}$) is ramped from 0V to 5.0 V. Eventually, one $I_{DS}$- $V_{GS}$ curves are overlaid using Tony Plot as depicted by fig. 4. DG NMOSFET. $V_{DD}$= -0.5 V was occupied to check the state-of-the-art at conduction, yet at low nimble field.

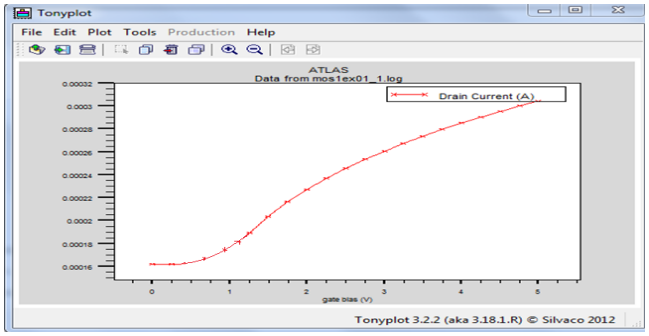


Fig. 3. The Id-Vgs curve for DGNMOS with $HfO_2$

### D. $I_{DS}$ versus $V_{DS}$ CHARACTERISTICS–

The curves manifest almost equal spacing for DG-NMOS transistor, stipulating a linear dependence of $I_D$ on $V_G$, instead of a quadratic dependence. It is also discerned that $I_D$ is not constant rather increases somewhat with $V_D$ in the saturation region. Fig. 5 depicts $I_{DS}$ versus $V_{DS}$ curves. For DG NMOSFET with $HfO_2$ as dielectric, gate voltage ($V_{GS}$) is set 0V, 50V & 80V and drain voltage ($V_{DS}$) changes from 0 V to 4.0 V by a voltage trek of 0.5 V.

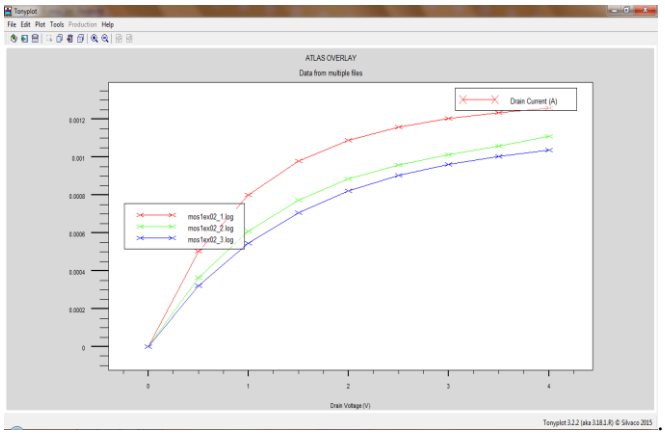


Fig. 4. Family of $I_d$-$V_{ds}$ curve for DGNMOS with $HfO_2$ as dielectric.

### E. SUB THRESHOLD VOLTAGE, $I_{OFF}$ AND $I_{ON}$ CURRENT-

The threshold voltage is the least possible gate-to-source voltage differential i.e. prerequisite to construct a conducting orientation between source and drain terminals [9]. Thus, $V_T$ is extracted when $V_{DD}$ equals -0.5V while gate voltage is ramped from 0 V to 5 V by a voltage trek of 0.5 V.

*International Journal of Engineering Applied Sciences and Technology*, 2016
**Vol. 1, Issue 4, ISSN No. 2455-2143, Pages 29-32**
Published Online January-February 2016 in IJEAST (http://www.ijeast.com)

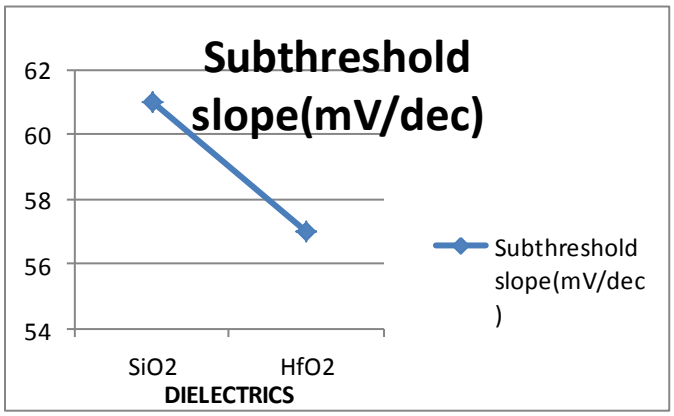


Fig. 5. Permutation in sub threshold cliff with divergent dielectric constant [8].

Transistor off-state current is marked as the drain current when gate-to-source voltage is nothing. Sundry aspects which predestine $I_{OFF}$ are $V_T$, channel substantial dimensions, channel doping profiles, drain / source solution depth and $V_{DD}$. From the characteristics it can be interpreted that there is an increment in on state current of the contrivance by wielding high k dielectric material [15]. Subsequently, the off-state leakage current of the DG-NMOS diminishes with the use of high k dielectric material, steering to high $I_{on}/I_{off}$ ratio of the device. $I_{off}$ diminishes as barrier potential increases. Here, $I_{ON}$ doubles for Hafnium oxide DG-NMOS in contrast to DG-NMOS with $SiO_2$ dielectric, thus substantial growth in the on state current is clinched. Moreover, minimum off state current is clinched for Hafnium Oxide DG-NMOS device.

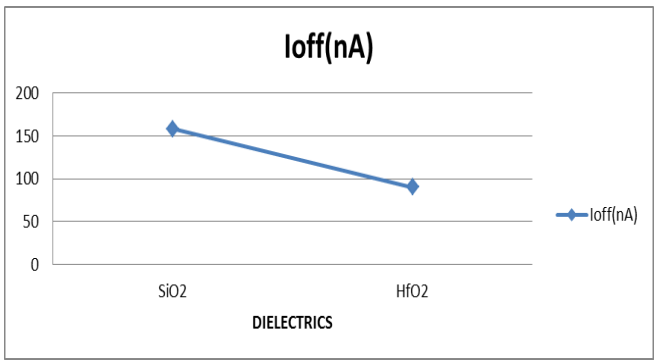


Fig. 6. Variation in $I_{off}$ with different dielectric DG-NMOS

The current which drift across source and drain when transistor is in the on-state, is known as $I_{ON}$. Take $I_{ON}$ at bias $V_{DD}$=-0.5 V and $V_{GS}$ =5.0V.

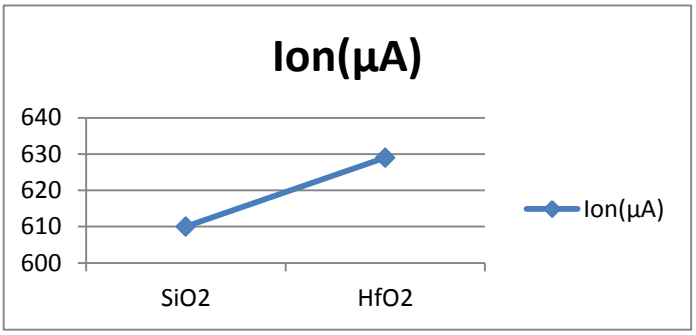


Fig.7. Variation in $I_{on}$ with different dielectric DG-NMOS

## III. RESULTS AND DISCUSSION

Delineating of DG NMOSFET wielding $HfO_2$ as dielectric by Silvaco TCAD tool at 35 nm is done and results have been presented. Subsequently results are compared in table 2 with DG-NMOS using $SiO_2$ as dielectric.

Table 2: Comparative analysis of DG NMOSFET with $SiO_2$ and $HfO_2$ as dielectric at gate length of 35nm

| DG NMOSFET | $V_T$ (V) | Sub $V_t$ Slope (mv/dec) | $I_{OFF}$ (nA) | $I_{ON}$ (μA) |
|---|---|---|---|---|
| DG NMOSFET with $SiO_2$ as dielectric | 0.107 | 61 | 158 | 602 |
| DG NMOSFET with $HfO_2$ as dielectric | 0.67 | 57 | 0.162 | 629 |

## IV. CONCLUSION

Delineating of DG NMOSFET wielding HfO2 as dielectric by Silvaco TCAD tool at 35nm is done and outcome are contrasted to Double Gate NMOSFET with SiO2 as dielectric. The device reliability is ameliorated and diminishing of Short Channel Effects has been discerned through the simulation repercussion. Planar edifice of DG MOSFET is the most propitious. Wielding high k dielectric material HfO2 leads to proliferating the on state current while the off state current, sub threshold slope and DIBL gets diminished, consequently device gets improved.

*International Journal of Engineering Applied Sciences and Technology,* **2016**
**Vol. 1, Issue 4, ISSN No. 2455-2143, Pages 29-32**
Published Online January-February 2016 in IJEAST (http://www.ijeast.com)


## V. REFERENCE

[1] H.-S. P. Wong, "Beyond the Conventional Transistor", IBM J. Res. and Dev. **46**, 133-168 (2002).

[2] Jean-Pierre Colinge, "Multiple-gate SOI MOSFETs", Solid-State Electronics **48**, 897-905 (2004)

[3] Jia-Liang Le, Zdenek P. Bazan and Martin Z. Bazant, "Lifetime of high-k gate dielectrics and analogy with strength of quasibrittle structures", Journal of Applied Physics **106**, 104-119 (2009).

[4] Hubbard, K.J., Schlom, D.G. "Thermodynamic stability of binary oxides in contact with silicon", J.Mater.Res. **11**, 2757-2776, (1996).

[5] Jean-Pierre Locquet, Chiara Marchiori, Maryline Sousa, and Jean Fompeyrine, "High-K dielectrics for the gate stack", Journal of Applied Physics **100**, 051-610 (2006).

[6] ShashanN , S Basak, R K Nahar, "Design and Simulation of Nano Scale High-K Based MOSFETs with Poly Silicon and Metal Gate Electrodes", International Journal of Advancements in Technology **1**, 252-261 (2010).

[7] Hui Zhao, Yee-Chia Yeo, Subhash C. Rustagi, and Ganesh Shankar Samudra, "Analysis of the Effects of Fringing Electric Field on FinFET Device Performance and Structural Optimization Using 3-D Simulation", IEEE Trans. on Electronics Devices **55**, 1177-1184 ( 2008).

[8] Saji Josepha, George James Ta and Vincent Mathew, "Transport characteristics and subthreshold behavior of High-K dielectric double gate MOSFETs with parallel connected gates", Journal of Electron Devices **16**, 1363-1369 (2012).

[9] Jae Young Song, Woo Young Choi, Ju Hee Park, Jong Duk Lee and Byung-Gook Park, "Design Optimization of Gate-All-Around (GAA) MOSFETs", IEEE Transactions on Nanotechnology **5**, 186-191 (2006).

[10] S. K. Mohapatra, K. P. Pradhan, and P. K. Sahu**,**"Nanoscale SOI N-MOSFETS with different gate engineering having biaxial strained channel - a superlative study" Journal of Electron Devices **15**, 1261-1268 (2012).

[11] "Sentaurus Structure Editor User's Manual", Synopsys International.

[12] International Technology Roadmap for Semiconductors (ITRS), 2007 Edition.

[13] M. J. Kumar, S. K. Gupta and V. Venkatraman, "Compact modeling of the effects of parasitic internal fringe capacitance on the threshold voltage of high k dielectric nanoscale SOI MOSFETs", IEEE Trans. on Electronic Devices **52**, 706-711 (2004).

[14] B. Corona, M. Nakano, H. Pérez, "Adaptive Watermarking Algorithm for Binary Image Watermarks", *Lecture Notes in Computer Science, Springer, pp. 207-215, 2004*.