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PERFORMANCE ANALYSIS OF FDSOI MOSFET FOR DIFFERENT METAL GATE WORK-FUNCTION

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Abstract— **Fully-Depleted Silicon Metal Oxide Field Effect Transistor is the prominent contender for sub micron regime.In this paper, the effects of work function on metal gate on the performance of FDSOI-MOSFET has been studied.Channel length that has been taken into consideration is 25nm.The parameters that has been investigated are transconductance, output conductance, on-current off current ratio, leakage current and electric field.Simulation results showed that by changing the work function of the metal gates of FDSOI MOSFETs threshold voltage of the device can be changed. By using this technique, threshold voltage of FDSOI MOSFET can be set at same voltage**.

Keywords—**MOSFET scaling, Very Large Scale Integration (VLSI), Fully-Depleted Silicon on Insulator (FDSOI), Partially Depleted Silicon on Insulator (PDSOI)**

I. INTRODUCTION

The future of electronics itself is the future of integrated circuits and electronics. Over the past thirty years, the growth of microelectronics, information sharing, signal processing has strongly dependent on very large scale integrated circuit industry. It all started with the insight of Lilienfeld of Insulated Gate Field Effect Transistor in 1925 which bore the potential to substitute the vacuum tube technology with small sized semiconductor transistor technology [1]. The first practical exhibition took place in 1960 by Kahng and Atilla in the form of the Silicon-based Metal Oxide Semiconductor Field Effect Transistor (MOSFET) [2]. In 1958, Jack Kilby at Texas Instruments conceived the idea of the Integrated Circuits(IC) and Robert Noyce from the Fairchild Corp. fabricated the first IC. The various advantages of integrated circuits have led to the development in many areas of science. According to Moore's Law, the number of transistors per chip in a dense integrated circuit has doubled approximately every two years [3]. Due to this, packing density of transistors per unit area is increasing in the VLSI microelectronic industries. This has been possible due to the comprehensive scaling, also known as miniaturization. The advantages of scaling are the speed improvements, increased packing density. The increased packing density has resulted in a chip with the same functionality in a lesser area, or chips with more functionality in the identical area. Also, the smaller ICs allow more chips per wafer, decreasing the price per chip. Silicon technologies have progressed faster in the past few years. The effects of reducing the dimensions of devices are the main issue that must be concentrated about the silicon technologies. The major device dimensions are the channel length, channel width and the oxide thickness. The reduction of channel length has led to the short channel effects. The shrinking of MOSFET device size has led to the degradation due to short channel effects in bulk device geometries.The reduction of channel length has degraded the device performance in terms of leakage current and short channel effects[4].To overcome the problem, a new circuit design technique has been developed such as Silicon-on-Insulator(SOI). Silicon on insulator (SOI) technology refers to the use of a layered silicon–insulator–silicon substrate in place of conventional silicon substrates in semiconductor manufacturing [5]. MOSFETs fabricated on SOI substrate that have a relatively thin SOI layer is known as fully-depleted SOI and for thick SOI layer is known as partially depleted SOI. In recent years, silicon-on-insulator has attracted considerable attention as an alternative substrate for low power application [6]. Because of BOX layer the fully-depleted silicon-on-insulator (FDSOI) has the advantages of lower parasitic junction capacitance and better sub-threshold swing, reduced short channel effects [7]. With the geometry scaling down to deep sub-micron range, the threshold voltage also scale down, therefore, threshold voltagr control is becoming more important for the future technology.

The SOI MOSFETs also suffer from short channel effects in the nano-regime due to reduction in threshold voltage [8]. Due to scaling of MOSFET threshold voltage is also decreasing. As a result, leakage current and short channel effects are also increasing. By providing the appropriate

gate work function, a metal gate technology can overcome these issues. Work function is the minimum energy (measured in electron volts) needed to remove electron from a solid to a point immediately outside the solid surface.

We can scale the traditional bulk MOSFET device structure down into the 10-nm gate length regime a heavy body doping will be required to control short channel effects because by using body doping we can reduce the depletion layer width of the MOSFET devices[9]. But the result is not comparable to the SOI MOSFET, and also this presents a challenge to the degradation of device fabrication. Even if we can achieve this, it will result in reduced carrier mobility and random dopants fluctuations.

We can also set the appropriate threshold voltage of SOI MOSFET device by providing channel doping and thin Si-film variation but it degrades the device performance in terms of SCE, carrier mobility and dopant fluctuations [10]. A large channel doping will also increase band-to-band tunneling leakage between the body and drain. As a result, both channel doping and Si-film variation result in degraded device performance. This emphasizes need for gate work function engineering as alternative solutions for nano meter devices. By using work function engineering we can change the threshold voltage of SOI MOSFET and we are able to maintain device performance and also able to get better results in terms of short channel effects and leakage current. Hence by altering work function of metal gate of SOI MOSFET, we can set the appropriate threshold voltage, and we are able to reduce the short channel effects and leakage current.

II. ADVANTAGES OF SOI OVER BULK TECHNOLOGY

SOI MOSFET has many advantages over the bulk MOSFET in device and circuit level. Because of the buried oxide (BOX) layer, the parasitic capacitances of SOI MOSFET devices are smaller than those of bulk MOSFET. Thus, the delays of digital CMOS circuit due to junction capacitances can be reduced by using SOI MOSFET, which therefore increase the speed of the digital CMOS circuit.In another aspect, the power delay product of SOI CMOS circuit is smaller as compared to the bulk counterpart, owing to the smaller parasitic capacitances in SOI MOSFET as well as reduced leakage currents through BOX. The SOI MOSFET has higher speed and low-power properties. SOI-MOSFET has no latch-up due to the buried oxide isolation and device isolation is much simpler for the SOI MOSFET as compared to the bulk-MOSFET, which make SOI CMOS technology a higher device density and an easier device isolation structure. Although these advantages of SOI technology are well known, the successful introduction of SOI technology for large–scale applications faces some challenges across the entire spectra of material, process, manufacturing, devices and designs. The SOI manufacturing processes are just becoming mature enough for mass production of low –cost, low-defect-density substrates. Another major concern is the control of silicon film thickness to accurately control the threshold of fully depleted devices. The SOI wafers potentially offer "perfect" transistor isolation (lower leakage), tighter transistor packing density (higher transistor count/higher IC function at the same lithographic resolution), reduced parasitic drain capacitance (faster circuit performance and lower power consumption), and simplified processing relative to bulk silicon wafers. Due to these advantages, SOI wafers appear ideal for leading edge integrated circuits with high speed, high transistor count, low power operation, and battery operated systems requirements, such as microprocessor ICs [11].

Silicon-on-insulator (SOI) wafers have traditionally been used for extreme environmental applications, such as high temperature and severe environments. However, they are expected to expand into mainstream CMOS applications due to these advantages:

- Faster device operation (speed/power product) due to reduction of parasitic capacitance (primarily due to reduced source-drain junction capacitance, but also from gate-to-substrate capacitance and metal-to-substrate capacitance).
- Lower power consumption (speed/power product) due to lower operating voltages on devices and lower parasitic capacitance.

III. SHORT –CHANNEL EFFECTS IN FDSOI-MOSFETs

A MOSFET device is considered to be short when the channel length is the same order of magnitude as the depletion-layer widths of the source and drain junction. As the channel length L is reduced to increase both the operation speed and the number of components per chip, the so-called short-channel effects arise [11].

A. Threshold Voltage of FD-SOI-

The analysis provided here is for NMOS, with its extension to PMOS device being straightforward. The threshold voltage of an n-channel MOSFET is classically given by [12]:

$$V_{th} = \emptyset_{MS} - \frac{Q_{SS}}{C_{ox}} + 2\emptyset_F + \frac{N_A\, x_{d\,max}}{C_{ox}} \quad (1)$$

where $\emptyset_{MS}$ is the work function difference between the gate and the channel and equal to $\emptyset_m$ - ($\emptyset_{Si}$-$\emptyset_F$). Q_{SS} is the surface state charge of the channel. C_{ox} is the gate capacitance and equal to $\frac{\epsilon_{ox}\epsilon_o}{t_{ox}}$. t_{ox} is the gate oxide thickness. $\emptyset_F$ is the Fermi potential, equal to $\frac{kT}{q}\ln(\frac{N_A}{n_i})$, where N_A is the channel

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doping concentration. x_{dmax} is the maximum depletion width. The threshold voltage for the fully depleted silicon on insulator devices changes to:

$$V_{th} = \emptyset_{MS} - \frac{Q_{ss}t_{ox}}{\varepsilon_{ox}\varepsilon_o} + 2\emptyset_F + q\frac{N_A t_{si} t_{ox}}{\varepsilon_{ox}\varepsilon_o} - Q_{ssb}\left(\frac{t_{ox}}{\varepsilon_{ox}\varepsilon_o} + \frac{t_{si}}{\varepsilon_{si}\varepsilon_o}\right) \quad (2)$$

where the Q_{ssb} is the surface charge between the silicon film and the buried oxide, t_{si} is the silicon film thickness.

B. Subthreshold Slope (SS) –

It indicates how effectively the flow of drain current of a device can be stopped when V_{gs} is decreased below V_{th}. When I_D-V_g curve of a device is steeper subthreshold slope will improve. Subthreshold slope is given by [13]:

$$S_t = \left[\frac{dV_{gs}}{d(\log_{10} I_{ds})}\right] = \frac{kT}{q}\left(1 + \frac{C_d}{C_i}\right) \quad (3)$$

C_d =depletion layer capacitance
C_i =gate oxide capacitance

C. Drain Induced Barrier Lowering (DIBL)-

In the weak inversion regime, there is a potential barrier between the source and the channel region. The height of this barrier is a result of the balance between drift and diffusion current between these two regions. The barrier height for channel carriers should ideally be controlled by the gate voltage to maximize transconductance. The DIBL effect occurs when the barrier height for channel carriers at the edge of the source reduces due to the influence of drain electric field, upon application of a high drain voltage [14] . This increases the number of carriers injected into the channel from the source leading to an increased drain off-current. Thus, the drain current is controlled not only by the gate voltage, but also by the drain voltage.

IV. DEVICE STRUCTURE

SOI refers to placing a thin layer of silicon on top of an insulator usually silicon dioxide or known as buried oxide (BOX) as shown in figure 1.SOI MOSFET can be further divided as partially depleted (PD) and fully depleted (FD) as shown in figure 2. For FD SOI device, the SOI layer is much smaller than the depletion width of the device and its potential is controlled by the gate. The advantages of the FD SOI MOSFET include the elimination of the floating-body effect and better short channel behavior. The better control of short-channel effects comes from the reduced source/drain junction depth, which increases the series resistance of the source/drain.

Furthermore, the requirement of silicon thickness smaller than depletion width results in a low device threshold voltage with high sensitivity to process and thickness variations.

For PD SOI device, the SOI layer thickness is thickness than the maximum depletion width of the gate.Usually, the silicon film thickness is more than 50nm, which alleviates the constraint on device threshold voltage and its sensitivity. Also, PD SOI device make the manufacturing easier and the process and the device design are much more compatible than with traditional bulk CMOS[14]. However, the major issue of the partially depleted device is floating –body effect and the resulting parasitic bipolar effect.

In general, PD SOI device is optimal for high speed and is being used for the applications where highest clock rates are needed. FDSOI device allows optimization for high temperature and extremely low power applications. FD SOI is considered as the best candidate for low noise RF microelectronics. RF figures of merit of FD SOI device such as cutoff frequency, maximum oscillation frequency, noise and transconductance are much better than bulk MOSFET and PD SOI MOSFET.Consequently, the SOI devices simulated and studied in this paper are FD SOI MOSFET, which are more likely to be used in RF CMOS circuit in next decade.

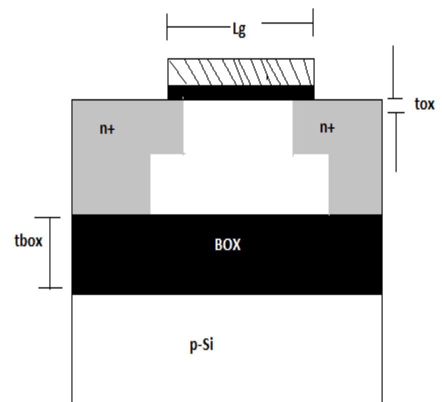

Fig. 1 Structure of SOI MOSFET

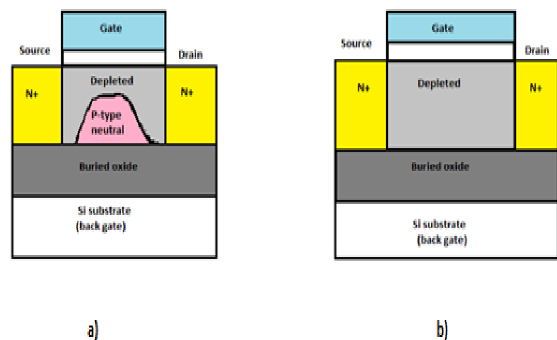

Fig.2 a) PD SOI MOSFET b) FD SOI MOSFET

Single gate Fully-Depleted SOI MOSFET structure is designed and simulated in this work.The structure is representative of well- scaled depletion-mode device at 25nm technology with substrate doping of boron $N_a = 1\times 10^{18}\,cm^{-3}$, channel doping with boron as $1\times 10^{17}\,cm^{-3}$ and source/drain doping with phosphorous $N_d = 1\times 10^{19}\,cm^{-3}$. General features of the device and other information are described as gate length= 25nm, thickness of gate oxide=0.7nm, buried oxide length= 35nm, nitride spacer length=2nm, thickness of spacer = 5nm, source and drain length= 5nm each as shown in Fig.3.

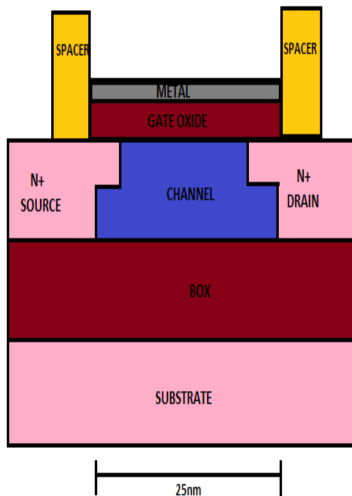

Fig.3 Structure for FDSOI-MOSFET

V. SIMULATION RESULTS

A. Transconductance g_m-

It measures the drain current variation with a gate-source voltage variation while keeping the drain-source voltage constant and is of crucial importance because it decides the ability of the device to drive a load. The transconductance has a important role in determining the switching speed of a circuit and voltage gain of MOSFET amplifiers. High transconductance devices yield circuits capable of high speed operation.
Transconductance of a MOSFET

$$g_m = \frac{\Delta I_{ds}}{\Delta V_{gs}} \quad (4)$$

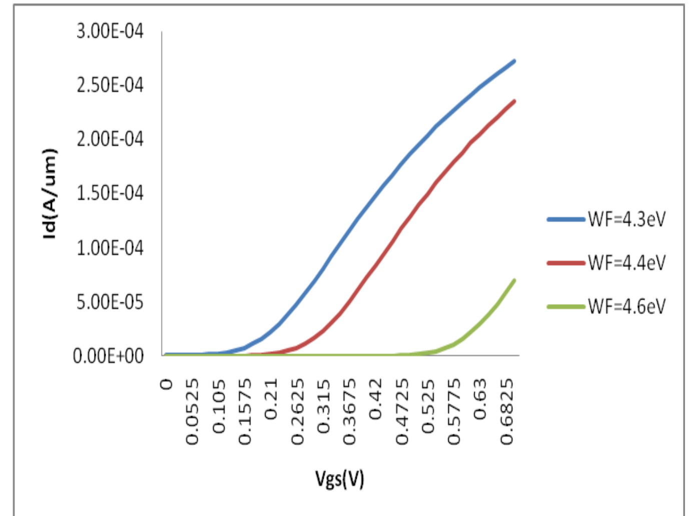

Fig.4. Drain Current as a function of gate voltage for different metal work function.

Fig.4.shows the drain current as a function of gate voltage for different metal gate work function.This curve indicates the transconductance of SOI MOSFETs at different work function of metal gate. As we decrease work function of metal gate transconductance of device increase. This is because from equation (2) as metal work function reduce threshold voltage reduces means at low gate voltage channel formed so drain current increase.

B. Output Conductance g_d-

It measures the drain current variation with a drain-source voltage variation while keeping the gate-source voltage constant.
Output conductance of a MOSFET

$$g_d = \frac{\Delta I_{ds}}{\Delta V_{ds}} \quad (5)$$

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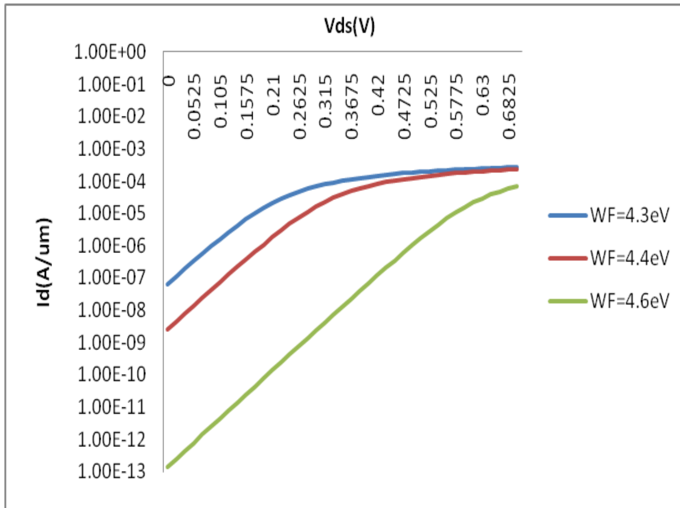

Fig.5. Drain Current as a function of drain voltage for different metal gate work function.

Fig.5. shows the gate leakage current variation with gate voltage at different function metal gate. As we increase the metal work function gate function gate leakage current decreases. From figure 5 it also examines that when we increase gate tunneling current increases.But after certain point it is saturated to a constant value.

C. On Current OFF Current ratio (I_{ON}/I_{OFF})

I_{off} is the current at the gate voltage at V_{ds}= 0V and I_{on} is the maximum current at the gate voltage $V_{ds} = V_{dd}$.

$$I_{on}/I_{off}=\log_{10}\frac{I_{on}}{I_{off}} \quad (6)$$

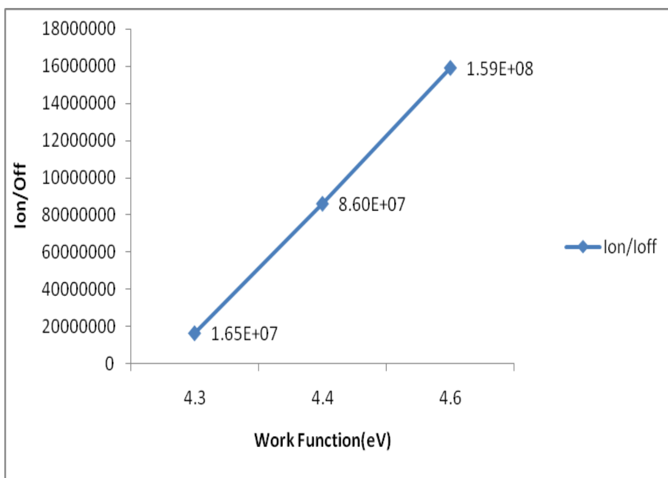

Fig.6 Ion/Ioff variation with metal gate work Function.

Device has higher value of on current to off current ratio provide high switching speed. Fig.6 shows the variation in Ion/Ioff with different metal gate work function. It seem s from figure that as we increase the work function of metal gate Ion/Ioff increases.

D. Leakage Current (Off Current) I_{off} -

At $V_{gs} < V_{th}$, an N-channel MOSFET is in the off-state. However, an undesirable leakage current can flow between the drain and the source. The MOSFET current observed at an N-channel MOSFET is in the off-state. However, an undesirable leakage current can flow between the drain and the source. The MOSFET current observed at $V_{gs} < V_{th}$ is called the subthreshold current.

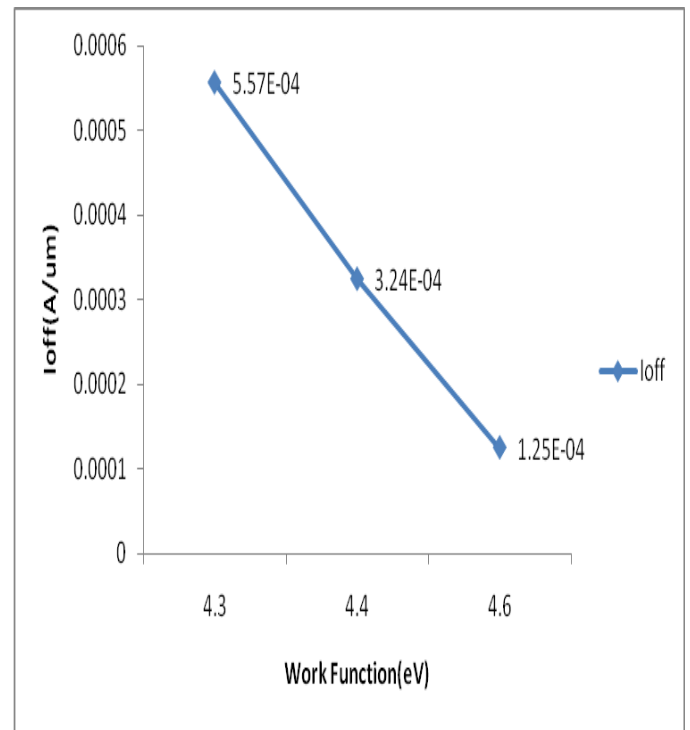

Fig.7 Leakage Current analysis at different different metal gate work function

Figure 7 shows the variation in leakage current as function of work function of metal gate. As the work function of the metal gate increases threshold voltage increase, the leakage current of SOI MOSFET decrease exponentially with threshold voltage.

E. Electric Field-

It is defined as the electric force per unit charge.It is the measure of intensity of electric field at a particular location.

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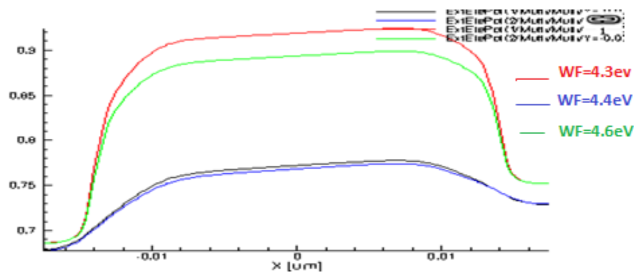

Fig.8 Vertical electric field Vs position along channel direction for different metal gate work function

Fig.8 shows the variation of electric field along the channel direction for different metal gate work function.From the curve it is clear that for lower values of work function of metal gate the vertical field along the channel direction is high.

VI. CONCLUSION

The device performance in terms of short channel effects and leakage current has been degraded with the continuous down scaling of MOSFET device.There is a need of device structure that provide better performance in sub-micron regime. Threshold voltage is decreasing with the reduction in the channel length scaling that increases leakage current and short channel effects.

Si-filmvariation and channel doping are the concepts by which we can set the desired value of threshold voltage, but it degrades the carrier mobility and dopant fluctuations.The work function engineering is the concept by which we can set the appropriate threshold voltage of SOI device. As we increase the work function the leakage current decreases so we choose a particular value of work function which provides better performance.From simulation it is concluded that at 4.4 eV metal gate work function SOI OSFET device shows better performance.In addition, metallic gates provide immunity from the depletion without affecting device performance. Hence, we can set the appropriate threshold voltage by changing the work function of metal gates of SOI MOSFET.

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