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A COMPARATIVE ANALYSIS OF BANDWIDTH ENHANCEMENT TECHNIQUES FOR TIA

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***Abstract*— This paper gives a comparative analysis of various bandwidth enhancement techniques intended for use in Transimpedance Amplifier (TIA) based on Complementary Metal Oxide Semiconductor (CMOS) technology used in optical communication. The CMOS technology in TIA has lower power consumption compared to other technology also it enables integration. The IEEE 802.3 standard provides 40 Gb/s and 100 Gb/s with multiple channels such as 4 channels of 10 Gb/s for 40 Gb/s. In this paper, various techniques such as series peaking, triple resonance network, π -type inductor peaking, g_m -boosting technique will be set side by side.**

Keywords—**Bandwidth (BW), π -type inductor peaking (PIP), triple resonance network (TRN), g_m- boosting, Regulated cascode (RGC) amplifier.**

I. INTRODUCTION

With the acceleration in the development of multimedia applications on the Internet, tens of gigabits per second is required to complete data transfers worldwide. Optical fiber technology has progressed due to the constant need for large data rates in many communication systems. The optical transceiver requires a high-efficient TIA for the front end of the receiver [1]. A transimpedance amplifier at the input stage amplifies the photocurrent received from the photodetector and converts this photocurrent to the output voltage according to the requirements of the receiver [2]. The performance of the transimpedance amplifier is calculated by several general consideration parameters, such as obtained bandwidth, transimpedance gain, sensitivity referred to noise current and supply voltage and power consumption [3][4]. Although high-bandwidth TIA designs utilizing Si/GaAs-bipolar technology [5][6] are particularly dominant, however, if low price is intended, the best option is the use of CMOS technology. CMOS technology has different advantages, for example, improving maximum operation frequency, reducing the power consumption and accomplishing more compact designs. A study on recent trends in CMOS technology has found that the two circuit topologies most commonly used for TIA design are common gate and shunt feedback. Some methods (bandwidth expansion techniques) have been implemented that use these topologies to increase the performance of a TIA such as a shunt peaking, series peaking, π -type inductor peaking (PIP), triple resonance network (TRN), gm- boosting. A TIA is designed to offer low input impedance to meet bandwidth requirements with high gain and low noise. In this article, these techniques are described from the point of view of their performance.

This paper, we make a comparative analysis of bandwidth enhancement techniques for TIA to understand best available techniques. The organization of this paper is as follows. Section II is about literature review of previous studies. Section III consists of comparative table of previous publication. Finally, Section IV draws the conclusion.

II. LITERATURE REVIEW

The purpose of this chapter is to review some past work in the field of BW enhancement techniques that have been noted in the literature to improve the performance of TIA. A portion of the strategies that have been concentrated in past are recapitulate below.

A. Shunt Peaking

It is well known conventional approach for improving bandwidth in wideband amplifier. In this approach, resonant peak is used in the output. Here, bandwidth is increased by attaching an inductor at output load which raises a resonant peak in the output level as the amplitude begins rolling down at much greater frequencies. This extreme technique increases the effective load impedance when the capacitive reactance falls at higher frequencies [7]. The structure of amplifier having shunt peaking [8] can be seen in Fig. 1.

A series connection of an inductor with resistive load forms a resonance circuit which minimizes the effect of the parasitic capacitances at transistor's drain and loading capacitance at next level stage. Thus, reduces the overall output capacitance. Kromer [9] has used this technique in 80nm technology node at all stages of the TIA. He achieves the transresistance gain of 52dB.Ω and 13GHz as 3-dB bandwidth where C_{PD} capacitance of photodiode he used to be 220fF.

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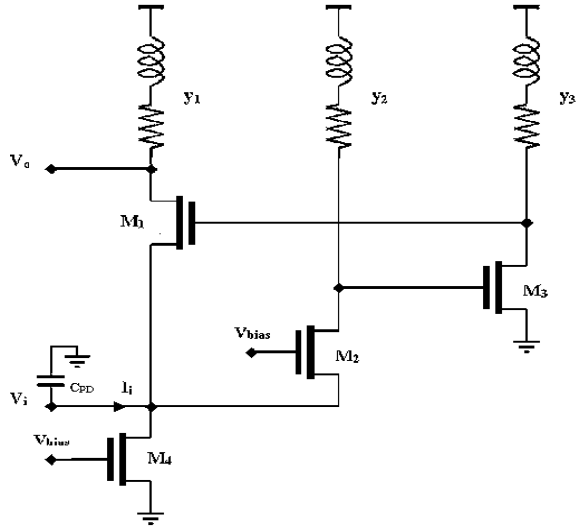

Fig. 1. Schematic of CG-TIA with shunt peaking by Kromer [9]

B. Series Peaking

This technique was presented in 2005 by Chia-Hsin Wu. Here, inductor is placed in series with every stage in the signal path of the multistage TIA, thus known as series peaking [10]. As shown in Fig. 2. these inductors are used to minimize the effect of parasitic-capacitance at different stages of the amplifier. In absence of inductor, BW for amplifier is usually calculated by RC-time constants of every node. The result was obtained in 0.18-µm CMOS profile, achieves a transimpedance gain of 61dB.Ω and bandwidth 7GHz. The value of capacitance for photodiode used to be 250fF. Wu presented the series peaking technique in 10-Gb/s CMOS-TIA to demonstrate the BW extension technique.

Further in 2010, Kim and Buckwalter [11] proposed a design for bandwidth enhancement with low group-delay-variation (GDV) with data-rate of 40 Gb/s. This TIA is outlined using 0.18-µm technology node in CMOS technology. Fig. 3. represents the circuit schematic consists of one TIA stage and two stage of postamplifier to mitigate GDV and to provide voltage gain. This research work demonstrates the 50 dB.Ω of transimpedance gain and 3-dB Bandwidth of 29 GHz with GDV is kept within 12 ps. The second work of Kim and Buckwalter [12] published in 2012 having push & pull shunt feedback amplifier followed by one postamplifier stage realized using 45 nm SOI CMOS technology at 40 Gb/s. Fig. 4. shows the circuit design where R_F is provided to determine minimum transconductance and L_2 is in series with two stages. This work provides transimpedance of 55 dB.Ω and 3-dB Bandwidth is extended to 30 GHz compare to previous publication on 40 Gb/s TIAs.

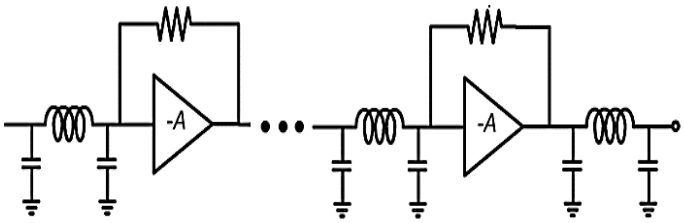

Fig. 2. Schematics of the 5-stage TIA using series-inductive peaking technique [10]

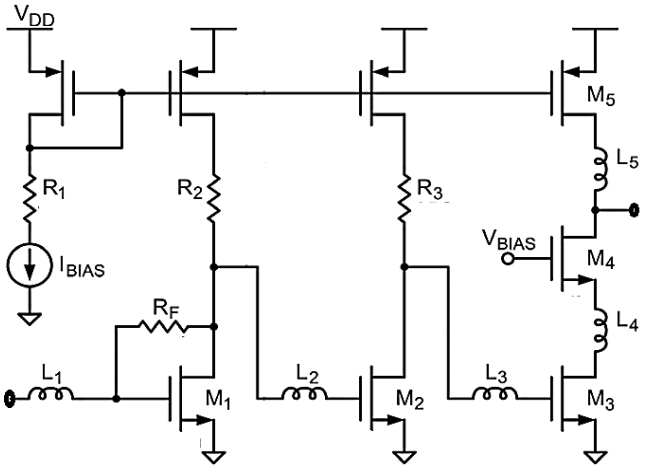

Fig. 3. Proposed TIA circuit [11]

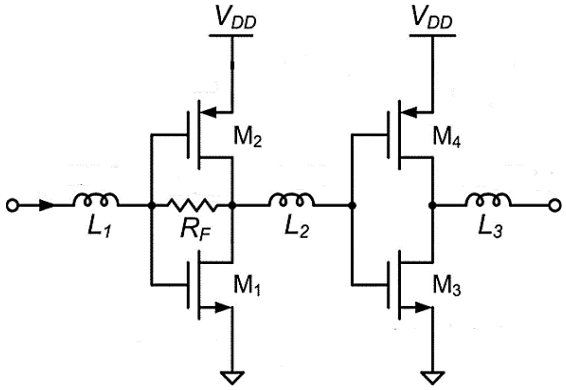

Fig. 4. Schematics of the TIA stage amplifier with postamplifier [12]

C. PIP Technique

This technique is proposed by Jin and Hsu [13] in 2008 to reduce the effect of parasitic capacitance using several combination of inductors. This several combinations of the inductor shape a Π like structure and known as a PIP. They designed TIA by implementing 4 cascaded CS stages with PIP topology to escalate the bandwidth. The Fig. 5. shows circuit implementation of combination of three inductors in a common source configuration. Fig. 6. Shows the small-signal equivalent circuit model of one gain stage with the PIP inductors.

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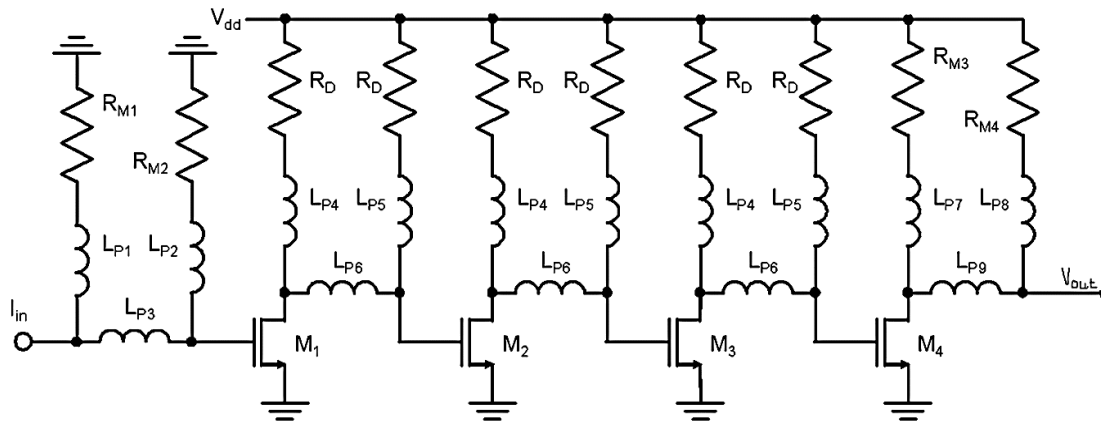

Fig. 5. Circuit implementation by Jin and Hsu proposed in 40-Gb/s Data Rate CMOS TIA using PIP technique[13]

This technology improves the TIA's BW by resonating with the devices' intrinsic capacitance. The CS stage is the elementary unit of the designed Wideband TIA. This design offers less GDV and minimum power consumption than other structure. The TIA's BW limit is resolved by PIP configuration and it is applied to resonate the photodiode's parasitic capacitance i.e. C_{PD}. This 40-Gb/s TIA is designed using technology node of 0.18µm CMOS-technology and results around 30.5 GHz of 3dB BW and 51dB.Ω of transimpedance gain. The value of C_{PD} here is 50fF.

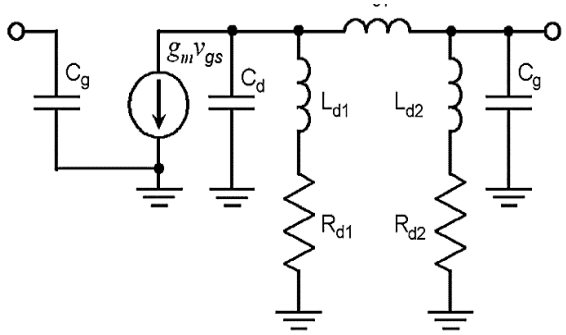

Fig. 6. The equivalent circuit model with PIP technique [13]

D. **Reverse TRN inductor peaking**

Liao and Liu present this technique in 2008 and design of 40 Gb/s TIA-AGC and CDR circuit using technology node 90 nm digital CMOS [14].The Mathematical equations were also calculated in this paper to simplify the architecture and scrutiny of RTRNs that showed a significant increase in BW by huge factor compared to earlier shunt and series peaking technique, particularly when the parasitic capacitance is ruled by next level. This TIA design incorporates RTRNs and -ve feedback in CG configuration. The amplifier uses shunt-feedback around an input stage of CG to minimize the input resistance while including RTRNs at the intersection between stages to expand the BW. In RTRN topology as shown in Fig. 7. , series RL branch are placed at output node rather than input node so that if C_1 and C_2 are unequal than L_1 and L_2 can be chosen to obtain a flat frequency response. This research work in 40Gb/s TIA demonstrates the gain value 60dB.Ω and 40 GHz as 3dB BW which is significantly high.

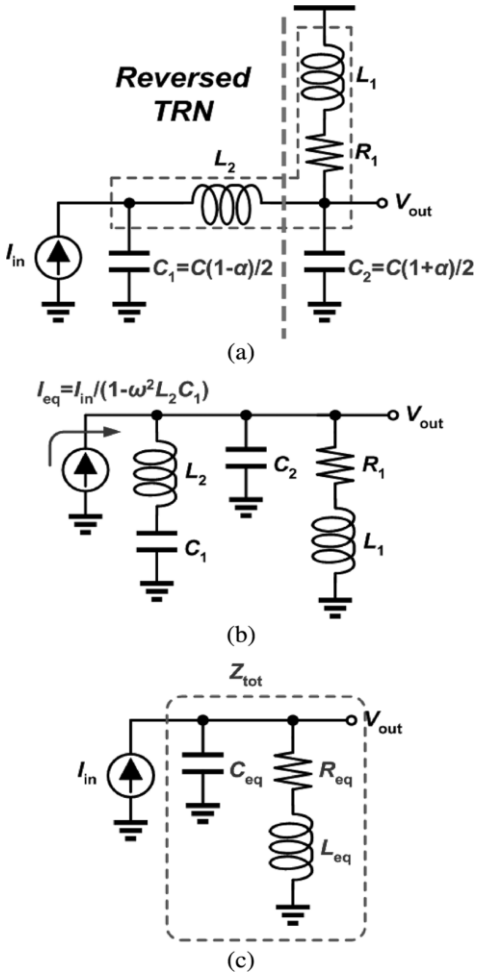

Fig. 7. (a) Design of RTRN. (b) Simplification of RTRN. (c) Small signal model of RTRN [ ].

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E. g_m-Boosting Technique

Bashiri and Plett (2010) proposed gm-boosting with the help of modified TIA-RGC configuration which enhances the bandwidth upto two times and minimizes the sensitivity(input current noise) and also take over the weakness of the RGC. This boosting technique upgrades the efficiency of RGC circuits without improvising speed. To provide small input resistance, transconductance g_m is boosted either by increasing width of M_1 of RGC-TIA amplifier or by increasing the bias current. But increasing width and current also creates anomaly in circuit such that width increases the input and output capacitances of M1 while current increases the input noise. Another way to minimize input resistance is by increasing gm_2R_2 [15]. This Fig. 8. shows the proposed RGC-TIA amplifier by Bashiri and Plett. This model by Bashiri and Plett is based on cherry-hopper technique to maximize the BW. Using cherry- hopper, resistance at output node and Node X is decreases due to R-L series feedback path and this decrease in resistance increases the frequency of M1, thus eventually increases the BW of the TIA.

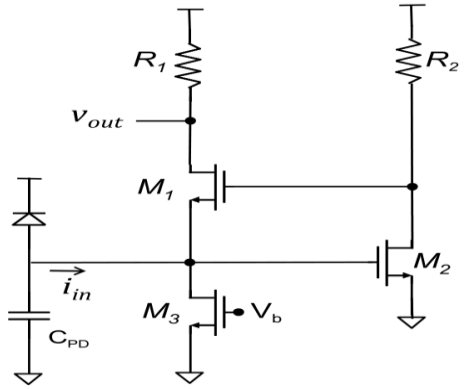

Fig. 8. Proposed RGC-TIA amplifier by Bashiri and Plett [15]

III. Comparison Table

The performance comparison of different TIA architectures is shown in Table 1 on the basis of their general considerated parameters.

IV. Conclusion

This paper shows advances in bandwidth-enhancement-techniques in CMOS-TIA regarding their designs concern and performance improvement. However, it is a challenge for designers to improve the satisfactory performance of all TIA parameters despite the rapid-progress in CMOS technology. Various peaking and circuit topology has been discussed in this paper. In general, techniques using inductor element in circuitry are quite common to enhance the bandwidth also researchers suggests that some areas in this chip may be lost for high data rates. But, this is a challenging task since we need to have fewer inductor to have low chip manufacturing cost.

V. Reference

[1]. García del Pozo, J.M., Serdijn, W.A., Otín, A. et al., "2.5 Gb/s CMOS preamplifier for low cost fiber-optic receivers,". Analog Integr Cir. Sig Process 66, 363–370 (2011).

[2]. U. Alvarado, G. Bistué, I. Adin, "Low Power RF Circuit Design in Standard CMOS Technology" (Springer, Berlin, 2011), p. 104.

[3]. Z. Lu, K.S. Yeo, W.M. Lim, M.A. Do, C.C. Boon, "Design of a CMOS broadband transimpedance amplifier with active feedback," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst*. 18,461–472 (2010).

[4]. Q. Gao, S. Xie, L. Mao, S. Wu, Y. Gu, H. Li, Q. Song, "A single-to-differential broadband transimpedance amplifier for 12.5 Gb/s optical links," *IEEE J. Solid-State Circuits* 14, 2(2017).

[5]. S. Kudszus, A. Shahani, S. Pavan, D.K. Shaeffer, and M. Tarsia, "A 46-GHz distributed transimpedance amplifier using SiGe bipolar technology," in *IEEE international MTT-S in Microwave Symposium Digest* (2003), pp. 1387–1390.

[6]. H. Zheng, R. Ma, M. Liu, "A 77-dB dynamic range low-power variable-gain transimpedance amplifier for linear LADAR,".*IEEE Trans. Circuits Syst*. *II* Express Briefs 65(2), 171–175(2018).

[7]. B. Analui and A. Hajimiri "Bandwidth enhancement for transimpedance amplifier," *IEEE J. of Solid-state Circuits*, vol.39, pp. 2334-2340, Dec (2003).

[8]. S. S. Mohan, M. D. M. Hershenson, S. P. Boyd and T. H. Lee, "Bandwidth extension in CMOS with optimized on-chip inductors," in *IEEE Journal of Solid-State Circuits*, vol. 35, no. 3, pp. 346-355, March (2000).

[9]. C. Kromer, G. Sialm, T. Morf, M. L. Schmatz, and F. Ellinger et al.,"A low-power 20-GHz 52-dB/s transimpedance amplifier in 80-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 39, no. 6, pp. 885–894, Jun.(2004).

[10]. C.-H. Wu, C.-H. Lee, W.-S. Chen, and S.-I. Liu, "CMOS wideband amplifiers using multiple inductive-series peaking technique," *IEEE J. Solid-State Circuits*, vol. 40, no. 2, pp. 548–552, Feb. (2005).

[11]. J. Kim and J. F. Buckwalter, "Bandwidth Enhancement with Low Group-Delay Variation for a 40-Gb/s Transimpedance Amplifier," *IEEE Trans. Circuits Syst. I Regul. Pap*., vol. 57, no. 8, pp. 1964–1972, (2010).

[12]. J. Kim and J. F. Buckwalter, "A 40-Gb/s Optical Transceiver Front-End in 45 nm SOI CMOS," *IEEE J. Solid State Circuits*, vol. 47, no. 3, pp. 615–626, (2012).

[13]. J.-D. Jin and S. S. H. Hsu, "A 40-Gb/s Transimpedance Amplifier in 0.18-um CMOS Technology," *IEEE J. Solid State Circuits*, vol. 43, no. 6, pp. 1449–1457, (2008).

[14]. C.-F. Liao and S.-I. Liu, "40 Gb/s Transimpedance-AGC Amplifier and CDR Circuit for Broadband Data Receivers in 90 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 43, no. 3, pp. 642–655, (2008).

[15]. S. Bashiri and C. Plett, "A 40 Gb/s transimpedance amplifier in 65 nm CMOS," in *IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 757–760, (2010).

Table 1. Performance comparison of different TIA architectures.

PARAMETERS	**COMPARISION OF DIFFERENT BW ENHANCEMENT TECHNIQUE**						
Publication Year and Reference	2004 [9]	2005 [10]	2010 [11]	2012 [12]	2008 [13]	2008 [14]	2010 [15]
BW Enhancement Technique	Shunt	Series	Series	Series	PIP	RTRN	g_m- Boosting
Z_T (dBΩ)	52	61	50	55	51	60	46.7
3-dB BW (GHz)	13.4	7.2	29	30	30.5	40	38
DC Power (mW)	2.2	70.2	45.7	9	60.1	75	39.9
Input refered noise (pA/$\sqrt{Hz}$)	50	8.2	51.8	20.47	55.7	22	30
Power supply (V)	1	1.8	1.5	1	1.8	1.2	1.2
Bit Rate (Gb/s)	10	10	40	40	40	40	40
Technology Node (nm)	80	180	130	45	180	90	65
C_{PD} (fF)	220	250	50	50	50	80	200