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# SEVEN LEVEL MODULAR MULTILEVEL CONVERTER WITH FFT ANALYSIS

Rakesh Gole
Department of EEE,
B.M.S College of Engineering,
Bengaluru, Karnataka, India

Dr.C.Lakshminarayana
Department of EEE,
B.M.S College of Engineering,
Bengaluru, Karnataka, India

**Abstract - The inverter is an electrical device that transforms direct current to alternating current, where the amplitude and frequency of the output voltage are regulated using an effective P.W.M. technique. The multi-level inverter has impressive benefits, and the latest research for single- phase application is discussed. The suggested topology is then built in this paper with a combination of a 3-level inverter for middling voltage application. The three level inverter portion, as created in a traditional 3-level inverter, eases the excluded positive and negative spikes. The proposed 7-level inverter efficiency is tested with RL load, and their findings are reported.**

**Keywords: 3-level inverter, multi-level inverter, modulation of the sine pulse width, middling voltage.**

## I. INTRODUCTION

The higher power value is derived from a series of low voltage inputs in multilevel inverters and the measured voltage output waveform above the sine wave is also integrated. The multilevel inverter has recently become popular for the use of renewable energy sources in vast amounts of power generations [1-4].to reduce the power and voltage spectrum for grid connected applications, the lower rating of photo voltaic and fuel cells can be directly combined with set. It helps control giant DC-link voltages with reduced device stress and reduced harmonics for utilization of higher level medium voltage.

The multilevel inverter design was developed with 3 simple topologies of (i) clamped neutral stage (ii) floating capacitor, and (iii) cascaded H-bridge inverter[5-8]. Such standard topologies manifest extreme efficiency and are specific to traditional applications of voltage. The inherent drawback, however, is variance in losses connecting the systems and encouraging more clamping diodes in N.P.C. flying capacitor gives more than 3 high output for the number of stages, however the problem of condenser voltage balancing is becoming . A separate auxiliary tension balancing circuit or control technique is required. Cascaded H-bridge inverter with asymmetric voltage sources gives higher output levels [9]. But, More switches are needed, a driven loop, and independent DC different Source. Each H-bridge and higher control complexity for higher performance.

Several new and hybrid topologies were built to resolve the standard topology problem [10-12]. A modern 3-phase 5-level inverter is added by combining a 3level ANPC inverter with a moving condenser module. A new control technique for controlling the Voltage of the moving condenser is also introduced [13]. An efficient, closed loop controller to coordinate the F.C.[15] Voltage is provide during transients. A three phase sic level inverter with two level inverter and 3 level F.C fusion is recently proposed for standard voltage applications [16]. Yet it requires erratic breakdown of DC-link voltages and more equipment to switches.

Therefore a new composition of a 3-level is used in this paper at the alternative DC-link to traditional 3-level inverter [17]. The unwanted negative spike at the positive voltage levels and positive spikes at negative voltage levels occurs in a traditional 3-level inverter. Within this topology the unwanted positive fluctuations in the output voltage are removed when alternating between negative and zero stages. The definition of the proposed topology is derived from ANPC of 5-levels [13] and an inverter of 5 levels for OEWIM drives [14]. With lower switching devices, the proposed three phase seven level inverter has inherent benefits of higher output voltage levels. In This topology, a three level inverter for 3 phase applications is integrated with an H-bridge FC circuit. In MATLAB/Simulink environment, the achievement of the built seven level inverter is assessed with various levels of modulation.

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## II. PROPOSED TOPOLOGY

Within this topology, an H-bridge FC circuit is combined with 3-level inverter for three phase applications. The achievement of the built seven level inverter is assessed in MATLAB/Simulink environment with modulation levels varying. The function of a three level structure and full bridge circuit is jointly dependent on a necessary voltage level being generated at the output.

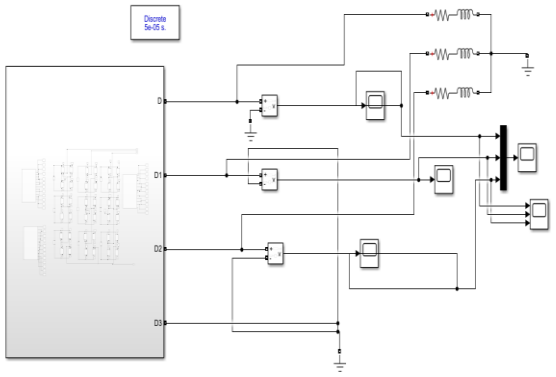

*Figure 1 : Proposed circuit topology.*

A single phase diagram of the proposed seven level inverter is seen at figure.2, to explain the process. A seven level inverter phase leg has 12 switches and 3 DC source of conflict. To generate the desired seven level output each source is connected to their H-bridge. The seven level inverter determines that the DC link capacitor share equal voltage. $S_{b4}$, $S_{b3}$, $S_{a3}$, $S_{a4}$ Switches have a lower voltage rating of $V_{dc}$ and $S_{a1}$, $S_{b1}$, $S_{a2}$ switches have a higher voltage level of $2V_{dc}$ and only $S_{b2}$ has a voltage rating of $4V_{dc}$.

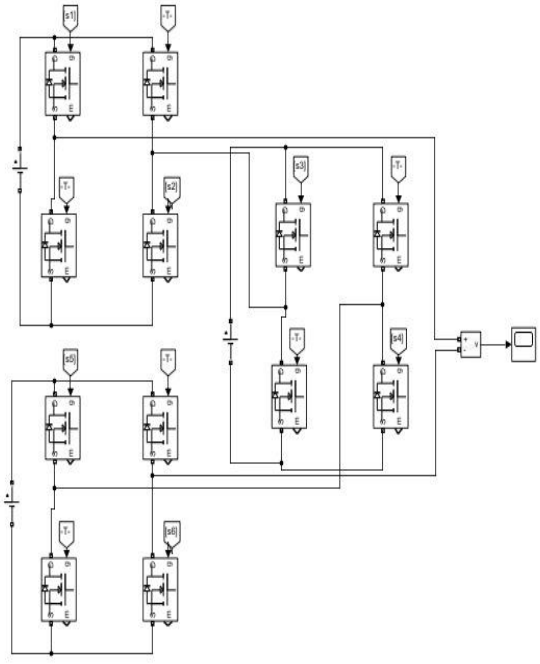

*Figure 2 : Simulation pattern for Single Phase inverter stage 7*

*Table 1 : Switching states of seven level inverter*

| **Switching states** | $V_{A0}$ | $S_{a1}$ | $S_{a2}$ | $S_{a3}$ | $S_{a4}$ |
|---|---|---|---|---|---|
| $V_0$ | 0 | 0 | 1 | 1 | 1 |
| $V_1$ | $V_{dc}$ | 0 | 1 | 0 | 1 |
| $V_2$ | $V_{dc}$ | 1 | 1 | 1 | 0 |
| $V_3$ | $2V_{dc}$ | 1 | 1 | 1 | 1 |
| $V_4$ | $3V_{dc}$ | 1 | 1 | 0 | 1 |
| $V_5$ | $-V_{dc}$ | 0 | 1 | 1 | 0 |
| $V_6$ | $-V_{dc}$ | 0(or)1 | 0 | 0 | 1 |
| $V_7$ | $-2V_{dc}$ | 0(or)1 | 0 | 1 | 1 |
| $V_8$ | $-3V_{dc}$ | 0(or)1 | 0 | 1 | 0 |

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Table-1 lists the seven level process line swapping states with inverter leg with the $V_{dc}$ stage. Where the transition states ON and OFF is marked by "1" and "0", respectively. $V_{AO}$ is the voltage of the pole which is then determined between the phase A and the neutral level. It should be understood that in $+V_{dc}$ and $-V_{dc}$ Voltage rates, there are two redundant switching states which affect the F.C. Voltage variously. The flipping state charges and discharges, depending on the direction of the phase current. The flipping notes that are $V_O$, $V_4$, $V_8$ has no effect on F.C. voltage and current does not pass through F.C.

Figure 3 shows displays existing directions for the different seven level inverter operating modes. The conductive switches and output voltage levels of the inverter are shown respectively in table 2, it should be understood that the number of conductive switches is very low for each stage. That ensures high efficiency for the proposed seven level inverter.

*Table 2 : Drive switches at various current Voltage Speeds*

| $Output\ Voltage\ Level(V_{A0})$ | Conducting Switches | Number of Conducting Switch |
|---|---|---|
| 0 | $S'_{a1}, S_{a2}, S_{a3,} S_{a4}$ | 4 |
| $V_{dc}$ | $S'_{a1}, S_{a2}, S'_{a3,} S_{a4}$ | 4 |
| $2V_{dc}$ | $S_{a1}, S_{a2}, S_{a3,} S_{a4}$ | 4 |
| $3V_{dc}$ | $S_{a1}, S_{a2}, S'_{a3,} S_{a4}$ | 4 |
| $-V_{dc}$ | $S'_{a1}, S_{a2}, S'_{a3,} S_{a4}$ | 4 |
| $-2V_{dc}$ | $S'_{a2},, S_{a3,} S_{a4}$ | 3 |
| $-3V_{dc}$ | $S'_{a2}, S_{a3,} S'_{a4}$ | 3 |

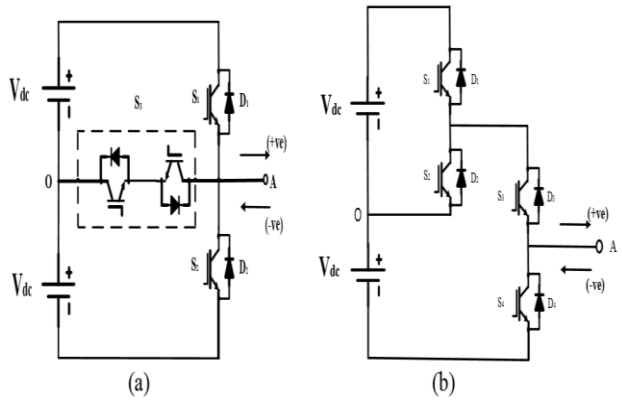


*Figure 4 (a) Regular three level inverter (b) Three level inverter proposed*

The efficiency of the device proposed is compared to a complete bridge F.C. And a three staged inverter [18]. In a standard three level inverter shown in figure.4 (a), while $S_{a1}$ is on $V_{A0} = V_{dc}$ , either of the two load current can be positive or negative when moving from $V_{dc}$ to "0", $S_{a1}$ has to be OFF, and then on a dead band of approximately 0.4μS, $S_{a3}$ will be ON. Each of the 0.4μS dead band, $S_{a3}$is ON, if the load current is +ve , then imposed to flow through the $D_2$ Diode , resulting in $V_{A0} = V_{dc}$, which is an unwelcome condition.

Switches $S_{a1} and\ S_{a3}$ conducts when$V_{A0} = 0$, $D_1$ and $S_{a3}$ conducts for zero voltage point in the proposed device in figures.4 (b), when $V_{A0} = V_{dc}$ , and load current is positive. When flipping from $V_{dc}$= 0, $S_{a2}$ should be off and $S_{a2}$ should be switched on after a dead band of 0.4μS. The positive load current flows into $D_2$ and $S_3$ during the dead band time even if $S_{a2}$ and $S_{a1}$ are off, since $S_3$ is not switched off, which will sustain the zero level during the dead band. If $V_{A0} = -V_{dc}$ is negative, and the load current is negative, then $S_4$ works . Does when $V_{A0} = 0$, $D_3$ and $S_{a2}$. $S_{a4}$ Should be off when transitioning from $-V_{dc}$ to nil and $S_{a3}$ should be switched on after the dead session, when $S_{a2}$ can be switched on automatically. Therefore, the negative charge current will pass through $D_3$ and $S_{a2}$ , maintaining the level of zero voltage. Clearly indicates positive exception, and negative fluctuations in the planned three level topology can be removed.

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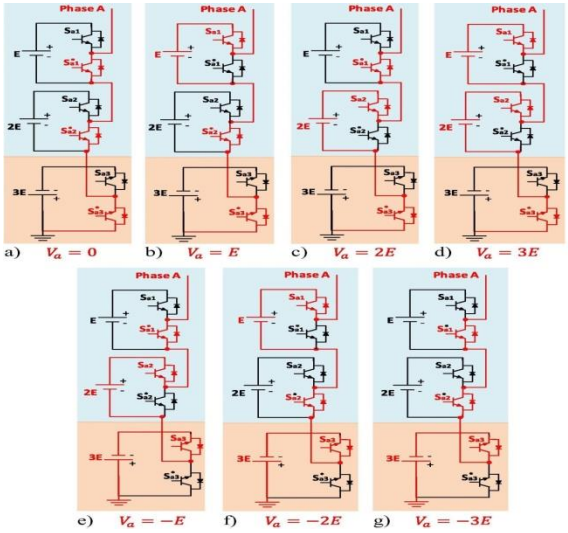


*Figure 3 : Modes of operation*

P.W.M. technique employed modulation of the disposition, as shown in figure.5. In this process, it is compared with the sinusoidal wave by using six carrier waves. Both carrier waves are moved and equal magnitude. The method used for switching is tri-phase modulation signals and (m-1) carrier signals. The frequency of the modulation signals is equal to the appropriate voltage output frequency. The carrier signals, on the other hand, have the same switching frequency, so the same amplitudes with a dc offset matches the carrier signal amplitude.

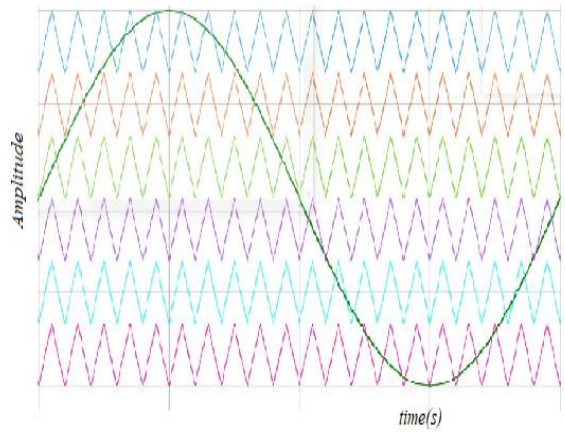


*Figure 3: SPWM*

## III. SIMULATION RESULTS

It was done in MATLAB / Simulink interface to check the performance of the suggested tri-phase seven-level inverter simulation work. For each H-bridge, the device parameters are of 110V voltage of 450Vrms. For the analysis the DC sources are analyzed to test the findings. The seven-level inverter is modulated using PWM for step disposal. The proposed inverter is capable of working at any charge inductance value. Used RL values are R=10Ω and L=0.5mH. Figure from (6 to 9) shows the different results in the proposed system as output phase voltage, tri-phase output voltage, tri-phase output voltage, FFT analysis and current.

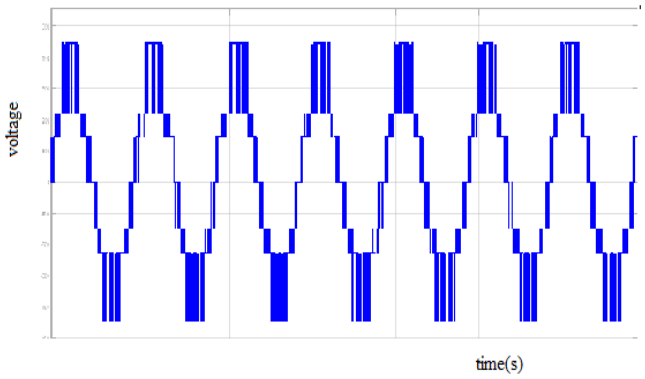


*Figure 4 : Phase Voltage*

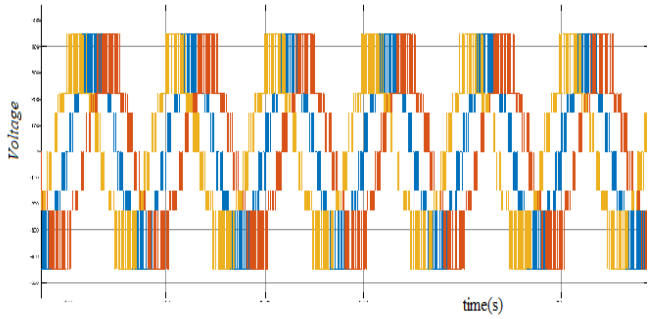


*Figure 5: line Voltages*

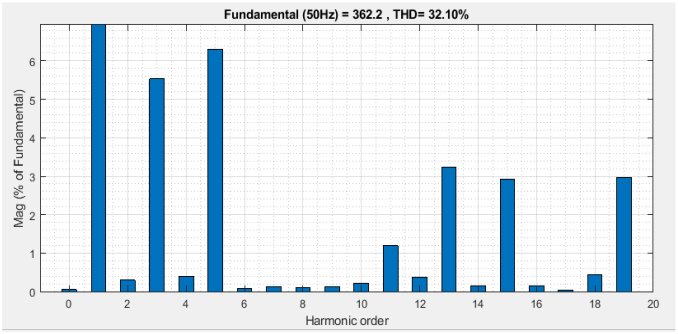


*Figure 6 : FFT analysis of seven level inverter*

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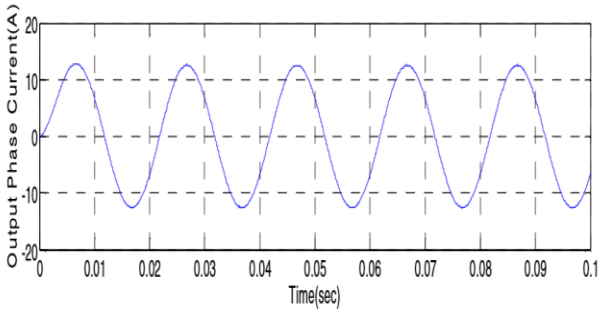


*Figure 7 : Current*

Figure 8, 9 and 10 shows the single phase voltage of a five level converter. For a five level converter only R-load is being used and the FFT analysis has been done. The focus of this comparison is to apply SPWM to symmetrical H-bridge inverter. Their related FFT analysis was performed for RL-load and R-load. The total harmonic distortion analysis of the below point reveals the modulating carrier frequency in Fc=4000Hz using PWM resistive load disposition process in step R=10 as follows

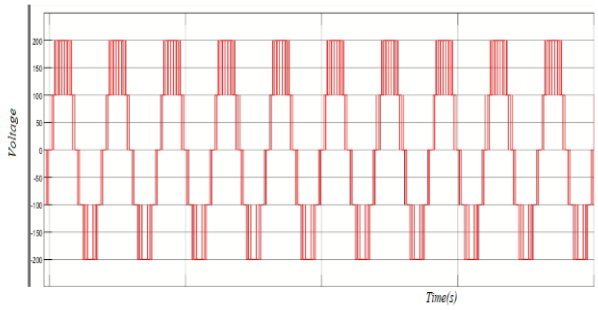


*Figure* ***8: single phase voltage of five level inverter***

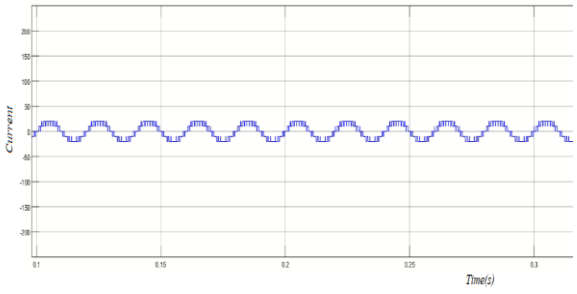


*Figure* 9 current waveform of five level inverter

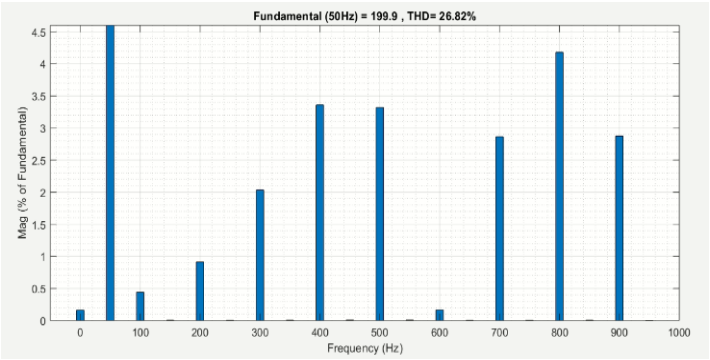


*Figure* 10 FFT analysis of five level inverter

## IV. CONCLUSION

A multi-level inverter with phase disposition PWM technique is proposed in this paper, which can be implemented in middle power applications based on renewable energies. The problem with this type of inverter is complexity and switch number. The proposed DC-link system is strong with specific output voltage (450V) and less THD (32.10 ) when compared to multilevel inverter . The seven-level inverter is evaluated using FFT analysis to assess the THD and the proposed device is simulated as a multi-level seven-level Simulink inverter in Matlab. The proposed design can be applied to applications with motor drive.

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