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A SINGLE-STAGE LED DRIVER WITH HIGH-PERFORMANCE PRIMARY-SIDE-REGULATED CHARACTERISTIC GUIDE

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Abstract—A traditional fly back LED driver is limited by its low performance, which usually does not reach the power factor (PF) and total harmonic distortion needed according to Energy Star or IEC61000-3-2. The control loop of the primary side from the secondary transformer has low reliability and employs more components, which reduces the power density of the system and increases cost. In this brief, based on single-stage single ended primary inductor converter (SEPIC) and fly back converter, a primary-side-regulated LED driver is proposed to improve the performance of the system. Working in DCM, the SEPIC circuit realizes the PF correction naturally. For the fly back converter, the proposed primary-side-regulated method improves the power density and guarantees accurate control of the output current. A 100-W prototype based on SEPIC-fly back was built to verify the analysis and the experimental results coincided with the analysis results satisfactorily.

Index Terms—High performance, LED driver, primary-side- regulated.

I. INTRODUCTION

Compared to traditional lighting sources, such as fluorescent and incandescent lamps, LEDs have their own unique advantages long working life, energy-saving, high illumination intensity, etc. Therefore, LEDs have been used in many applications, such as general lighting, LCD backlight, decorating lights and so on. In order to ensure good performance of LEDs, a highly efficient and reliable LED driver with constant current output is indispensable. In small and medium power applications, the fly back converter is a popular topology because of its simplicity and isolation characteristic [2]. To satisfy the demand of PF and THD according to IEC 61000-3-2 and Energy Star, a front stage PFC circuit is necessary.

For the PFC cell, there are many converters that can be used as PFC circuits, such as Buck, Boost, Buck-Boost, SEPIC and others. Buck converter is a step-down circuit, which is suitable for low output voltage loads instead of a high step-down ratio transformer [3]. However, it does not work in the whole half-cycle period, which means the PF is not close to unity. As for the Boost converter, it commonly functions as a PFC cell [4], but its step-up characteristic increases the backward voltage stress. In this brief, the SEPIC converter is selected to operate as a power factor corrector. One reason is that the SEPIC converter has two inductors at the input and output ports. The input inductor can cancel the filter components and limit the ripple of input cur- rent, which can be determined through the design procedure. Further, when working in DCM, the PFC function can be achieved naturally. The integration of SEPIC and fly back circuits can also satisfy the demands of IEC61000 and Energy Star. Therefore, the SEPIC is a desirable circuit to be used as a PFC cell.

In order to improve the reliability and increase the power density of the system, a primary-side control method is an attractive choice [6]. This brief presents an integrating capacitor method to solve the ringing effect in the auxiliary winding. A differential amplifier is used to improve the detection accuracy for the secondary-side working time, tDIS. In addition, a mirror capacitor is used to obtain a more precise peak current value. Therefore, the output current can be controlled more precisely compared to the traditional primary-side control method reported in [7]. The performance of the system has been verified by experimental results.
The single-stage topology based on SEPIC-fly back is show in Fig. 1. Next, the primary-side-regulated principle is discussed

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in Section II. The design of the LED current estimator cell and sample and hold (S&H) cell. Section IV presents the experimental results of the laboratory-made prototype.

II. PRIMARY-SIDE REGULATING

PRINCIPLE AND CHALLENGES:

The single-stage LED driver contains the SEPIC PFC cell and fly-back DC-DC converter cell. As depicted in Fig. 1, the SEPIC cell consists of two inductors L1, L2, two capacitors C1, C2, two diodes D5, D6, and one shared switch Q. As for the fly-back converter cell, it contains a transformer T, a diode D7, and a shared switch Q. The overall structure of the proposed system including the control scheme.

A.SEPIC PFC CELL:

For the SEPIC PFC cell, the voltage Vin(t) is the rectification of input voltage vin(t). As shown in (1), Vm is the amplitude of Vin(t) and ω is the angular frequency.

$$Vin(t) = Vm|\sin(\omega t)|$$

Then, the current iL1 through inductor L1 andthe current iL2 through inductor L2.Here, L1 and L2 are the inductors in the SEPIC circuit and Vin2 Leq i0 is the initial value.When iL1 = iL2 = i0, the current through diode D6 is zero.

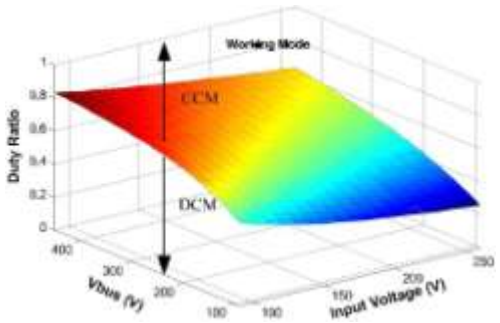
Thus, the turn-on time tD6 of diode D6 can be calculated

Here, Vbus is the voltage of bus capacitor C2, D is the duty ratio and Ts is the switching period. At the same time, the current through diode D6 reaches the peak value. The peak current ip d6 of D6. Here, Leq is the equivalent inductor of L1 and L2, where Leq = L1L2/(L1 +L2).

Therefore, the average current of diode D6 in the half switching period.

The average current through the primary inductorLp is equivalent to the output current of the SEPIC circuit, assuming that the efficiency is 100%; in other words, the input power equals the output power provided to the fly-back circuit. Eq. (6) shows the relationship between Pin and Pfly.

B. FLYBACK DC-DC CONVERTER CELL:



To ensure that the SEPIC circuit works in DCM, the working mode should satisfy (11) which means that the current through diode D6 is zero during a time interval at the end of the switching cycle. Here, tON is the switch turn-on time and tOFF is the time of D6 current changing from peak value to zero when the switch turns off.

$$Ts > tON + tOFF$$

the DCM or CCM condition. The input voltage is from 90 Vac to 260Vac and Vbus ranges from 90V to 450V according to the bus capacitor rated voltage. Below the 3-D surface, the SEPIC circuit works in DCM to result in the PFC function. The CCM working mode operates in the opposite direction.

C. PRIMARY-SIDE-REGULATED CELL:

Next, the LEDs load current will be discussed. The current ILED is the average value of iD7, which is the current of the secondary-side diode D7. When the switch is turned off, the energy in the secondary-side inductor, which comes from the primary inductor Lp, discharges to the LED load. When the current through diode D7 is zero, the primary inductor produces a quasi-resonance with the switch parasitic capacitance. to result in less energy loss, the switch is turned on. The current through the LED, ILED, has the following relationship with current iLs through diode D7. where Ts is the switching period and iLs is the current of the secondary inductor.

According to the transformer turns ratio n, the relationship between the peak current of the primary inductor iLp, peak and the current of the secondary inductor iLs. From (15), in order to accurately get the value of ILED, the detecting components are the peak current iLp, peak and the discharging time tDIS of the secondary-side diode.

III. ILED ESTIMATOR CELL AND SAMPLE AND HOLD DETECTION CELL

A. TDIS DETECTION CELL DESIGN

According to (15), two elements need to be measured: iLp,peak and tDIS. The detection circuit of tDIS is proposed the integrating capacitor Caux is used. To generate a suitable detection signal Vaux by filtering the Vaux signal of the transformer auxiliary winding. A ripple free measurement voltage Vaux can be obtained .The capacitance Cdelay and the resistance Rdelay are used to shift the voltage Vaux , thus generating the signal delay. Compared with the solution based on a hysteresis comparator, an accurate end instant tDIS can be generated by using a differential amplifier, which outputs the difference between Vaux and Vdelay. The main working principle is explained in next paragraphs.

Vaux can quickly reach the valid threshold voltage Vvalid which can be identified by the zero-crossing comparator. When the voltage Vaux changes from negative to positive, the zero- crossing comparator will output a high voltage Vstart. Then, through the NAND gate, a signal sets the RS trigger to recognize the start instant of tDIS.

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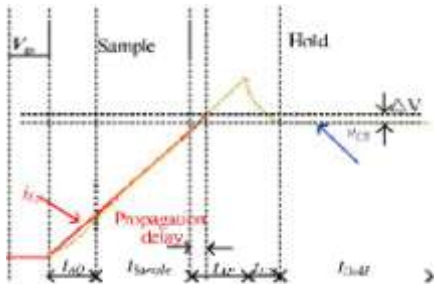


The traditional sample-hold circuit suffers from one serious drawback: when the circuit is during the holding period, the holding capacitor CH will discharge through the parasitic capacitor Cgd of the switch, rendering an inaccurate value of iLp,peak. This drawback can be overcome by introducing a mirror capacitor CM.

The main working principle is stated as follows and the main waveforms as given.

a) Sample period time: switch SW1 is turned on, while switch SW2 is turned off. The input signal Vcs goes through the Buffer to capacitor CH. The Buffer can accelerate the sample speed.

b) Hold period time: switch SW1 is turned off, while switch SW2 is turned on. The charge of capacitor CH dis-charges to the Gate-Drain capacitor Cgd. Meanwhile, the mirror capacitor C will offset the loss of energy from capacitor CH.

Capacitor CH is located in the feedback loop so it can not be influenced bt the output signal. Furthermore , the charge of CH can also be offset by the mirror capacitor CM. Therefore, the hold periods time will present a small error;in other word ,the detection peak current iLp,peak is nearly close to the true value .In addition ,can accelerate the acquisition speed.

IV. EXPERIMENTAL RESULTS

A 100 W single-stage LED driver based on the SEPIC and Flyback converter prototype has the high precision and performance of primary side regulated method. The main characteristics are started as the end instant of Tdis is the moment of the quasi resonant.

(1)Input voltage Vin= 22

(2) sin(100πt) =22

Start up, so Vaux will slowly decline. Shifting Vaux, Vdelay can be obtained .A differential amplifier is used to detect the difference between Vaux and Vdelay. This way as soon as the quasi resonant begins the differential amplifier can output the signal Vend better than the hysteresis voltage delay. A comparison between the hysteresis comparator and differential voltage waveforms.

(3) iLp, PEAK DETECTION CELL DESIGN

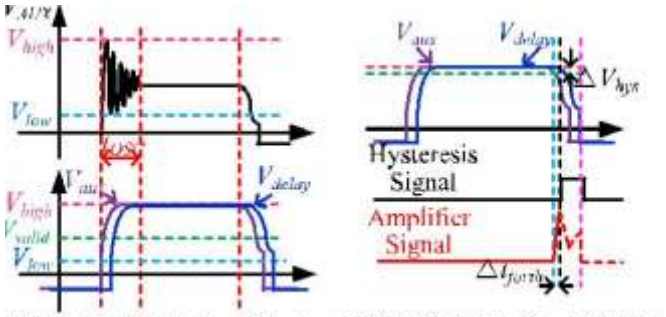
An accurate value of the peak current iLp, peak

(2) input current ripple Irip/Iin=25%

(3) working frequency Fs=100KHz

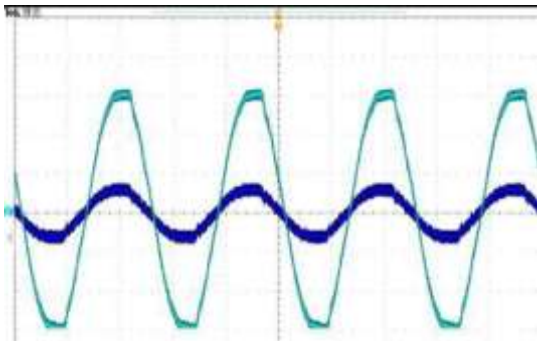
(4) output voltage Vo=50 V

(5) System efficiency is 90% at the rated 220Vacoutput voltage and the input voltage is 111W,where the ripple of the input current is set to be 25% of the input current and the duty ratio is set to be D=0.3. From (9) Leq can be obtained and the inductors can be calculated where Vin(t0) is Vm*sin(60). Vin(t0) DTs improved the precision control



(a) The Start Point of t_{DIS} Detection (b) The End Point of t_{DIS} Detection method.

L1 =Irip= 5.01 mH



Input Current and Input Voltage Waveforms.

For the selection of output capacitor C3, the value of capacitor C3 can be selected as per equation (18), where fline is the line frequency and Vo is the ripple of output voltage. The value of C3 is selected to be 68μF to decrease the ripple of output voltage. In order to improve the system efficiency, the flyback is operated in DCM, so that when the secondary-side current is zero, the quasi-resonance (QR) begins. According to the power expression. Then, the turns ratio of primary-side and secondary-side is set to be 36:8. The secondary-side inductor Ls of the transformer.

The capacitor C1 is calculated as (21), where ωr is 5%~10% of the switching frequency fs. So C1 is set to be 220nF.

Here, Q is 7N60B, D6 and D7 are F8L60.

The input voltage and current are shown in Fig. 7. As observed, the input current follows the input voltage perfectly. When the PFC cell SEPIC circuit works in DCM, the PFC function can be achieved.

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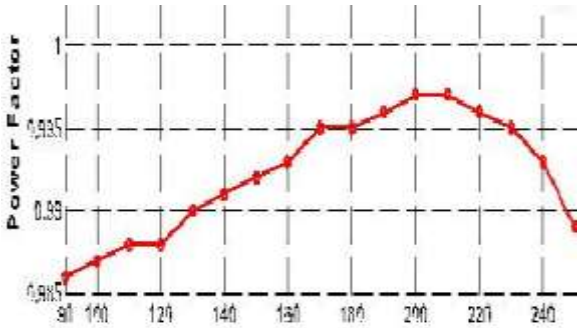
The PF and efficiency are shown in Fig. 8, when the input voltage changes from 90Vac to 260Vac. As shown in Fig. 8, the PF is always higher than 0.95 and the efficiency is also higher than 85%, with a maximum value of 90.8%. shows the PF and THD as the output power changes from 10% to 100%. The results satisfy the requirements of IEC61000-3-2. Input voltage, compared with the IEC61000-3-2 standard. The experimental results are lower than the corresponding standard limits.

To decrease the turn-on loss of the switch, QR method is adopted. As depicted, the turn-on voltage is relatively low to restrict the loss.



Power factor at different input voltage

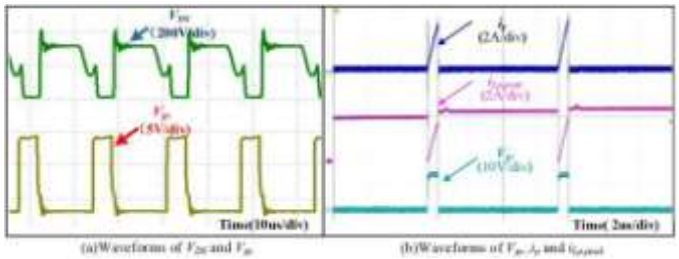
Input-current harmonics compared with IEC61000-3-2 class C standard.

To decrease the turn-on loss of the switch, QR method is adopted. The driver signal and drain-source voltage, Vds waveforms . As depicted, the turn-on voltage is relatively low to restrict the loss.

The peak current through the primary inductor Lp is detected by the proposed method shown in Fig. 11(b). As seen from Fig. 11(b), the detection point can be offset by the mirror capacitor.

tDIS is also a main detection parameter, which includes the start and end instant detection. The start instant is the start time of secondary-side working time shown in Fig. 12 (a). The end instant is the start time of quasi-resonant period shown in Fig. 12 (b). Fig. 12 (a) shows how the integral capacitor can overcome the ambiguous vibrating voltage. Fig. 12 (b) demonstrates how a differential amplifier can rapidly show the interval end point better than a comparator because the hysteresis comparator still persists the time-delay. Therefore, it is demonstrated how through the presented scheme the detection of tDIS is more accurate.

The current of ILED can be estimated by detecting the two main elements: ILp,peak and tDIS as mentioned in (15). Next, using the peak current control method, comparing the corresponding voltage Vcs of peak current. With corresponding Vfb of Iled ,the turn OFF time can be obtained .the proposed estimator can reach a better accuracy than reported.



Voltage and current signals during switching period

V. CONCLUSION

In this brief, an integrated-stage LED driver with primary-side-regulated characteristic is proposed. To better detect the start instant of the secondary-side working time t_{DIS}, an integrating capacitor is utilized. Moreover, a differential comparison method is proposed to capture the end instant of the secondary-side working time with high accuracy. In addition, to improve the precision of the sampled current, a novel sample-hold circuit has been developed. As a result, the power density and reliability of the system are improved by using primary-side-regulated method. The proposed methodologies have been experimentally verified by a 100W laboratory prototype, which showed high power factor, low input current distortion and an efficiency as high as 91%. In the future, with the increase of the working frequency of power MOSFETs, the primary-side-regulated method can further help to boost the power density of this kind of systems.

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